Ultra-Thin Chip Fabrication and Assembly Process

Martin Zimmermann, Wolfgang Appel, Joachim N. Burghartz, Saleh Ferwana and Christine Harendt

Abstract—**In this paper a new ultra-thin chip fabrication and assembly process is presented. During a pre-process module Chipfilm™ wafer substrates are prepared with extremely narrow buried cavities. In contrast to the established wafer thinning technique, the overgrowth of porous silicon membranes using a standard silicon epitaxy process precisely defines the chip thickness *a priori*. After CMOS integration on those dedicated wafer substrates chips are detached from the wafer surface in the Pick, Crack&Place™ post-process module. Trenches are etched along the chip edges into the buried cavities and the residual anchors fixing the chips at the wafer surface are cracked by applying a mechanical force. The feasibility of the new process is demonstrated through a mixed-signal circuit having 38,000 digital and 2,700 analog transistors.**

Index Terms— **Flexible electronics, integrated circuit technology, novel packaging concepts, porous silicon, ultra thin chips.**

I. Introduction

THE industrial demand for ultra-thin silicon chips increases from year to year. The applications of these ultra-thin chips basically fall into two categories, i.e. three-dimensional integrated circuits (3D IC) [1], [2] and systems-in-foil (SiF) [3], [4]. 3D ICs require dense through-chip vias (TCV) and thus very thin chip layers to reduce both TCV pitch and via parasitics [5]. Such an arrangement of vertically alternating active devices and interconnect layers can favorably be employed for an effective reduction of the average wire length in an integrated system, thus overcoming the bottleneck of increasingly dominant interconnect delay with miniaturization in planar ICs [6]. For SiF, the other category of thin-chip applications, the excellent mechanical properties of ultra-thin silicon enables the integration in a flexible package like foil or textile. For both application categories a cost efficient process technology for the fabrication of extremely thin chips with excellent thickness control is needed.

Industrially manufactured microchips are produced on wafers of 500 µm to 800 µm thickness. At the end of the manufacturing process they are thinned to approx. 200 µm and diced into individual chips. When silicon wafers are thinned to a thickness smaller than 150 µm they loose their rigidity. Hence they have to be attached to handle wafers or foils for mechanical support during the standard post-process steps to avoid breakage [7]. Furthermore, wafers that are thinned down from about 700 µm to approximately 20 µm using grinding techniques are obviously prone to thickness non-uniformity and generation of crystalline damage, leading to a varying chip thickness and a decreasing yield [8]-[10]. However, functional devices and circuits on chips having a thickness of ~20 µm and below have been demonstrated by using such wafer thinning techniques [9],[11].

In this paper we present and discuss a fundamentally new, cost efficient process for the fabrication and assembly of ultra-thin silicon chips where thinning and sawing of the wafers after the chip fabrication is not necessary [12]. Whereas conventional wafer thinning and chip dicing are post processes, the new technology here consists of a pre-process module "Chipfilm™" and a post-process module "Pick, Crack & Place™". This means that the majority of the additional process steps are applied to the starting wafer substrates instead of to the costly CMOS wafers. The definition of the final chip thickness during the pre-process module using an epitaxial overgrowth of porous silicon membranes leads to an excellent thickness control of the chips on the entire wafer. In Section II we describe the new concept in detail and discuss the associated advantages and challenges. In Section III we give evidence of the feasibility of the new technology. Finally, in Section IV, some conclusions are made.

II. The Chipfilm™ and Pick, Crack&Place™ Process Modules

In our new thin chip fabrication technology conventional starting substrates are replaced by pre-processed wafers that have buried cavities within the dedicated chip areas (Fig. 1a). Those pre-processed Chipfilm™ wafers are introduced to CMOS device integration like any conventional bulk substrate with the sole difference that a coarse alignment of the CMOS features to the dedicated chip areas needs to be arranged by using a zero-level alignment mark. After the CMOS fabrication is completed trenches are etched at the periphery of the chip areas down into the buried cavities, while leaving small anchors to the bulk substrate at selected places, such as the chip corners (Fig. 1b). The trench etching thus leads to a transition from strong connections between chip and bulk

Manuscript received October 1, 2008.

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wafer along the entire perimeter to a weak attachment only at those anchor points. The anchors are designed to be sufficiently strong for keeping the chips reliably in place during wafer handling but weak enough to allow for breaking off the chips by reasonable mechanical force. Therefore, a conventional pick and place assembly tool can be employed to attach a vacuum chuck to the chips, break off the anchors and transfer the chips to their packaging destination. Evidently, this post-process is called Pick, Crack&Place™ (Fig. 1c).

A. Details of the Chipfilm™ pre-process module

During the first process step global alignment marks are etched into conventional, low doped *p*-type wafers. Using ion-implantation into the wafer front- and backside the right boron concentration for the following anodic etching is set near the wafer surface (Fig. 2a).

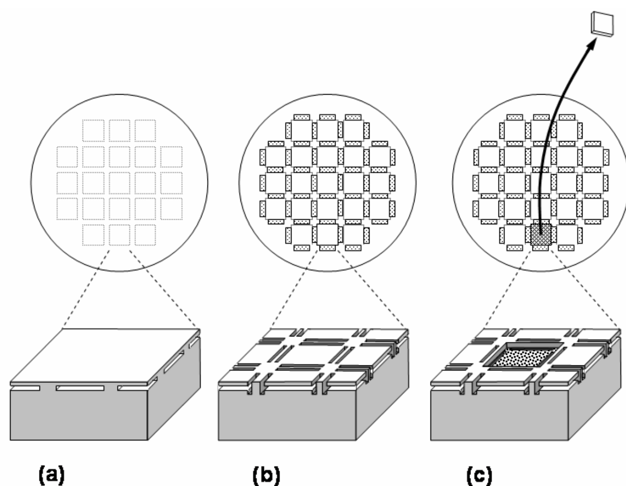

Fig. 1. Schematic illustration of (a) the Chipfilm™ pre-process module for preparing wafer substrates dedicated to thin-chip fabrication, (b) CMOS circuit integration followed by trenching leaving the thin chips only attached through selected anchors, and (c) detaching the thin chips by using a Pick, Crack&Place™ process to break the anchors and transfer the chips to the package.

N-type regions are formed through a lithographically structured implantation of phosphorous ions followed by an annealing step to protect from buried cavity formation, as will be explained next (Fig. 2b). In the following anodic etching process, a two-step process is carried out to produce dual layer porous silicon within the *p*-type regions (Fig. 2c). The *n*-type regions are not attacked by the anodic etching process because the current assisted etching of the silicon requires the presence of holes, and thus a *p*-type doping [13]-[17]. As a result of this two-step etching a ~1μm thick fine porous layer resides over a ~200 nm thin coarse porous layer within the chip areas (Fig. 2c; Fig. 3a). The *n*-type doped frame therefore serves as a chip separator, similar to the conventional dicing channels. Next, an annealing at 1100 ºC in hydrogen is applied, which leads to sintering of the porous silicon layers (Fig. 2d). Sintering means, that the porous silicon, having a very large surface area, transforms into a material with cavities featuring a minimum integral surface area [12], [15], [16], [17]. As a result, the fine porous layer transforms into micro/nano cavity-rich single-crystalline silicon, while the coarse porous layer converts to a ~200 nm narrow, continuous cavity (Fig. 2d;

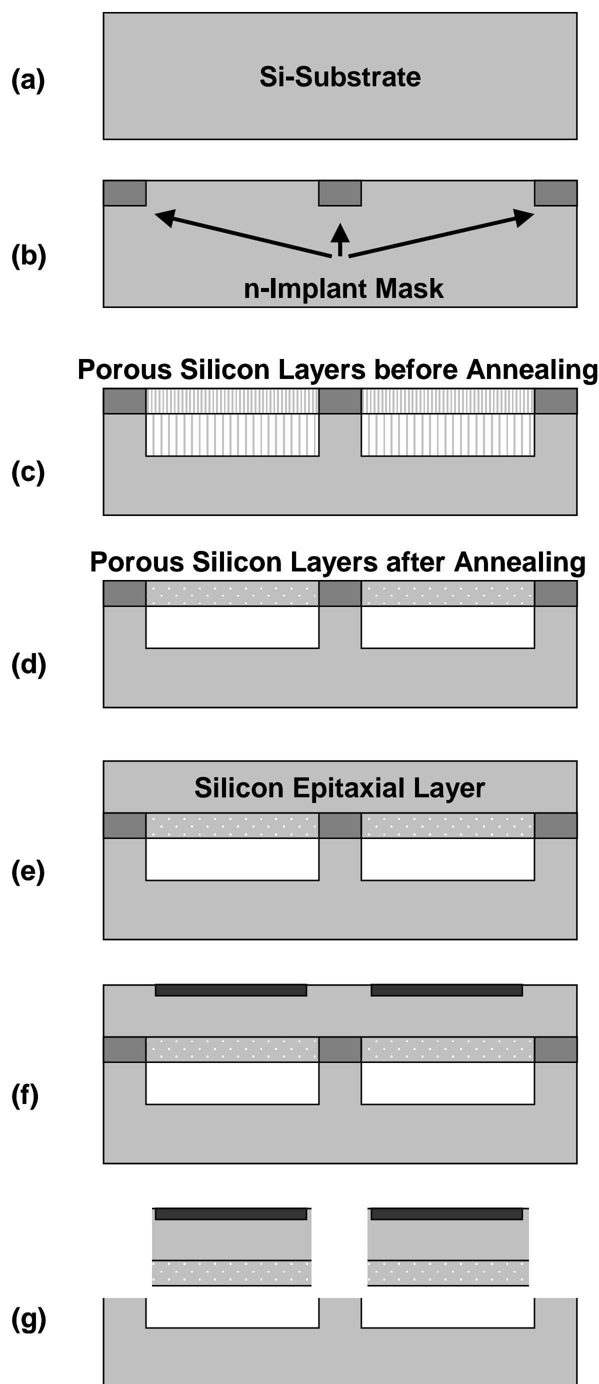

Fig. 2. Schematic illustration of the Chipfilm™ process flow: (a) starting *p*-type substrate (heavily Boron doped at the wafer surface), (b) with n^+-implant mask, (c) after dual-porous silicon etching within chip areas resulting in a 1 μm fine-porous over a 200-nm coarse-porous layer, (d) after sintering in hydrogen resulting in a ~1 μm thick micro-cavity rich silicon layer and a 200 nm buried continuous cavity, (e) after epitaxial overgrowth with device-quality silicon (typically 20 μm), (f) after CMOS integration above the buried cavities and (f) after trench etching at the chip edges down into the buried cavity leaving only anchors in selected places.

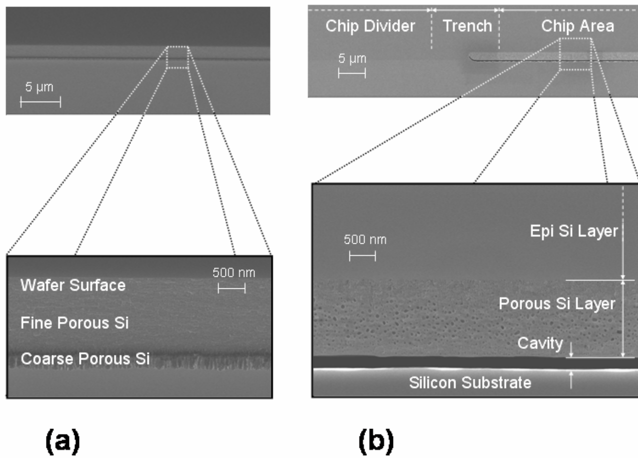

Fig. 3. Cross-sectional Scanning Electron Micrograph (SEM) of (a) the dual-porous silicon region at the wafer surface and (b) the buried cavity with above the micro-cavity rich silicon layer and the device-quality epitaxial layer, shown near the chip edge with indication of the position of the subsequent trench formation.

Fig. 3b). That cavity ends at the *n*-type chip separators (Fig. 3b). The fine porous silicon very close to the wafer surface closes during sintering, thus providing a uniform silicon surface with minimum topography (Fig. 3b). This surface layer features an excellent seed for the subsequent epitaxial device layer growth, which is carried out at 1100 ºC in $SiHCl_3$ at atmospheric pressure (Fig. 2e; Fig. 3b). The epitaxy layer essentially defines the thickness of the chip and provides device quality single-crystalline silicon for CMOS integration [12]. Those pre-processed Chipfilm™ wafers with mono-crystalline silicon membranes with a certain thickness above buried cavities are introduced to CMOS device integration and can be handled during the standard ASIC fabrication like any conventional bulk substrate.

B. *Details of the Pick, Crack&Place™ post-process module*

After CMOS device and interconnect fabrication trenches are etched at the chip edges leaving laterally silicon bridges to the bulk substrates in place (Fig. 2f). These trenches are positioned so that they reach down into, or more likely past the narrow buried cavity. The chips are then held in place by those silicon bridges, featuring anchors from the bulk substrate laterally to the chip edges. The chips are now in weak attachment to the substrate and can be broken off the wafer (Fig. 1c). This is done by using a pick and place tool, having a vacuum chuck to attach to the thin chip to both break it off and provide mechanical support. This support is maintained until the chip is mounted into a package or onto a flexible substrate, meaning that the chip is kept in a flat, supported state during the entire Pick, Crack&Place™ chip separation and assembly post-process. Without this support the chips would warp, particularly if they are very thin, due to tensile/compressive stresses in the silicon and the deposited layers thereon.

III. Device and circuit fabrication and characterization

For demonstration and evaluation purposes test devices and circuits were fabricated by using an in-house CECC-certified 6-inch, 0.8 µm CMOS gate array technology. The CMOS fabrication process is based on a *p*-well concept and has one poly and two metal layers. Both Chipfilm™ wafers with 20 µm thick mono-crystalline silicon membranes above buried cavities and reference bulk wafers were used in the same fabrication process.

A mixed-signal (38,000 digital and 2,700 analog transistors) circuit was fabricated on both bulk and Chipfilm™ wafers to demonstrate the feasibility of the

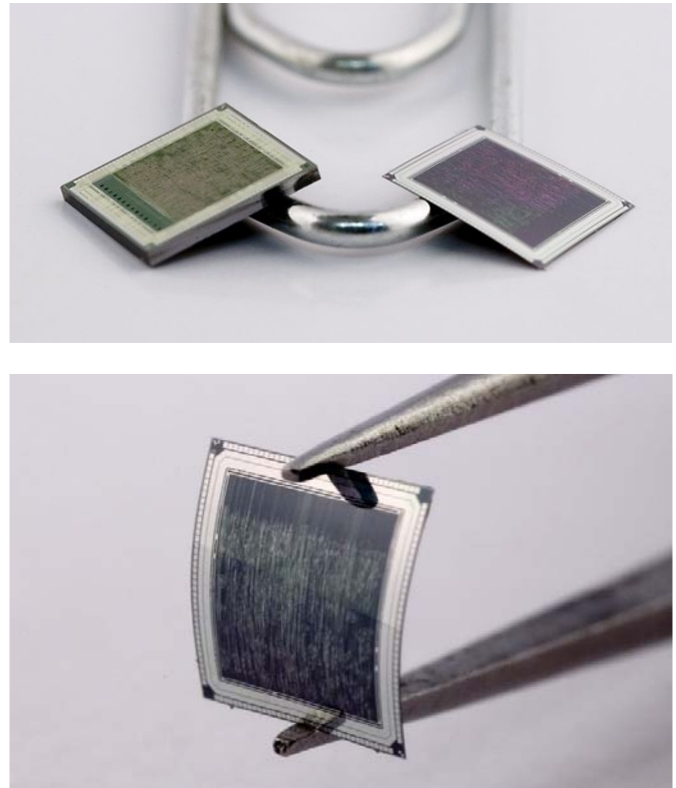

Fig. 4. Photo of a 20 µm thin test chip (a) in comparison with a conventional microprocessor chip and (b) photo of a clamped test chip illustrating its excellent mechanical properties.

Chipfilm™ and Pick, Crack&Place™ process modules (Fig. 3). For both bulk and Chipfilm™ samples electrical tests on wafer level and device characterization in ceramic packages were carried out, providing information about the device parameters and parameter variations as well as the mixed-signal circuit parameters. The characteristic device parameters derived from statistical on-wafer measurements on bulk and Chipfilm™ wafers are listed in Table I [18]. The minor deviations in the average electron and hole mobilities may be a result of the different wafer substrates used (p^+-Si, 14 mΩ-cm with 6 µm thick *n*-type epi layer for Chipfilm™ and n^+-Si, 25 - 50 mΩ-cm with 6 µm thick *n*-type epi layer for bulk control wafers). The fact that even slightly higher mobilities were observed on the Chipfilm™ wafers shows, that a planar

	Chipfilm™	Bulk Control	Difference
μ_n (cm^2/Vs) (9x0.8 μm^2)	Mean = 633 σ = 10.7	Mean = 607 σ = 9.4	+4.3%
μ_p (cm^2/Vs) (12x0.9 μm^2)	Mean = 178 σ = 4.03	Mean = 174 σ = 2.1	+2.3%
$L_{eff,n}$ (μm) (0.8 μm)	Mean = 0.79 σ = 0.018	Mean = 0.8 σ = 0.097	-1.25%
$L_{eff,p}$ (μm) (0.9 μm)	Mean = 0.82 σ = 0.021	Mean = 0.825 σ = 0.1	-0.6%
$V_{th,n}$ (V) (9x0.8 μm2)	Mean = 0.87 σ = 0.0058	Mean = 0.87 σ = 0.005	0
$-V_{th,p}$ (V) (12x0.9 μm2)	Mean = 0.917 σ = 0.0044	Mean = 0.915 σ = 0.0044	0
T_{RO} (ps)	Mean = 310 σ = 6	Mean = 300 σ = 6	+3.3%

Table I Statistical (mean values, standard deviations σ) CMOS transistor parameters (electron mobility μ_n, hole mobility μ_p, effective gate length L_{eff}, threshold voltage V_{th}) and ring oscillator delays for Chipfilm and bulk control wafers from on-wafer measurements.

and defect-free silicon surface was successfully regained with the epitaxial overgrowth of the sintered porous silicon regions.

IV. Conclusions

It can be concluded that the new thin-chip fabrication technology, involving the pre-process module Chipfilm™ and the post-process module Pick, Crack&Place™ presents a unique alternative to the established post-process wafer thinning techniques for fabricating ultra-thin silicon chips. In particular, the wafer pre-process Chipfilm™ allows for low-cost fabrication of ultra-thin chips with very accurate thickness control. The post-process Pick, Crack&Place™ is compatible with conventional pick and place tools and provides mechanical supported of the ultra-thin chips at all stages of the chip fabrication and assembly process. System-in-foil and three-dimensional ICs based on the chip-to-wafer concept appear to be very favorable applications for this new technology.

Acknowledgment

The authors wish to acknowledge E. Penteker, N. Remmers, E. Angelopoulos, C. Reuter, H. Rempp, H. Richter, S. Schmiel, I. Schindler, P. Vöhringer and in particular the staff of the IMS process line for support in device and circuit fabrication and characterization. Moreover, O. Tobail, M. Schubert and J. Werner from the Institute for Physical Electronics (ipe) at the University of Stuttgart are acknowledged for helpful discussions and support with porous silicon etching.

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