

# Millimeter-Wave Low Noise Amplifier in 90nm CMOS

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**Abstract**—This paper presents a 77GHz low noise amplifier (LNA) designed in a 90nm CMOS process. A three stages implementation realizes an acceptable power gain with limited transistor maximum available gain (MAG) in the 77GHz regime. The three amplifier stages are coupled by on-chip resonant-tuned transformers, which also act as inter-stage matching network. Simulation predict an overall power gain of 10.5dB. The input and output impedances are matched to 50Ω, with a return loss better than -10dB between 75.4 and 82.9GHz. From 75 to 87GHz, the noise figure is less than 4dB. Noise figure reaches the device minimum noise figure at 80GHz with value of 3.5dB. The input  $IP_3$  is -1.5dBm with two frequency tones applied at 76.5GHz and 77.5GHz. The -1dB compression point is -10.8dBm. At normal operation, the LNA draws 18.5mA from a 1V supply. The stability factor (K) is larger than 4 and  $\Delta$  is smaller than 1 between 100MHz and 200GHz, showing that the amplifier is unconditional stable.

**Index Terms**—Millimeter-wave, Amplifier, Noise, Matching, Transformer, 77GHz

## I. INTRODUCTION

Millimeter-wave (mm-wave) low noise amplifier will find potential applications in 60GHz broadband wireless local area networks with gigabit-per-second data transfer rate [1] and 77-79GHz automotive collision avoidance radar for future intelligent vehicle control system [2, 3]. Historically, mm-wave circuits are fabricated using gallium arsenide (GaAs) or indium phosphide (InP) materials, which are 3 or 5 times more expensive than silicon. With the continuous scaling of CMOS devices, the transistor transit frequency ( $f_T$ ) and minimum noise figure ( $NF_{min}$ ) will become competitive with the GaAs or InP counterparts. In the mm-wave regime, the short wavelength allows the implementation of on-chip antenna [4, 5]. This simplified the interconnection between the antenna, receive pre-amplifier and transmit power amplifier. Realization of mm-wave circuits in CMOS technology enables the integration of digital signal processing blocks and transceiver front-end on the same chip, allowing further reduction in the system cost and size.

The proposed block diagram of an mm-wave direct conversion receiver front-end is shown in Fig. 1. It consists of an on-chip differential antenna, two single-ended LNA, an on-chip balun transformer [6] and a double balanced mixer with on-chip local oscillator (LO) generator. The differential antenna receives the wireless signal and it drives two single-ended LNA. The LNA provides adequate power gain

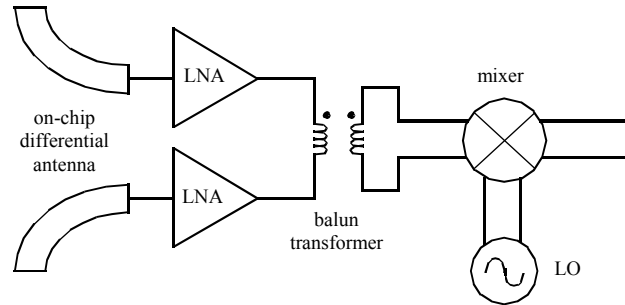


Fig. 1 Generic mm-wave direct conversion receiver front-end

to suppress the noise contribution by the on-chip balun, receive mixer and subsequent base-band circuits. The LNA must also have low noise figure and high linearity to enhance the receiver dynamic range. The on-chip balun combines the two output signals from the LNA and drives a double balanced mixer.

This paper presents the design of the single-ended 77GHz LNA as shown in Fig. 1. The LNA is designed in a 90nm digital CMOS technology. In the 77GHz regime, the NMOS transistor's MAG is typically less than 5dB. In order to realize an acceptable power gain, a practical implementation consists of three stages. Simulation results predict an overall power gain of 10.5dB and a noise figure of 3.5dB. The input -1dB compression point is -10.8dBm for a supply voltage of 1V and current consumption of 18.5mA.

## II. CIRCUIT DESCRIPTIONS

The schematic of the LNA is shown in Fig. 2. It consists of three amplifying stages. The first stage is optimized for low noise figure and power matched to a 50Ω antenna. It is an inductively degenerated common source amplifier  $M_1$  and  $L_{s1}$ .  $M_1$  consists of 20 fingers with each finger width of 1μm. Double gate contacts are placed at both ends of the finger to lower the gate resistance and thus to maximize the available power gain and minimize the noise figure.

Source degeneration ( $L_{s1}$  of 90pH) improves the amplifier linearity and provides a 50Ω real part of the input impedance which eases the design of the input matching network. A small inductance in the order of 100pH could be implemented as a single turn coil using the top metal layer. A 0.8V was chosen for the gate bias ( $V_b$ ) as a compromise between the transistor's minimum noise figure and MAG.

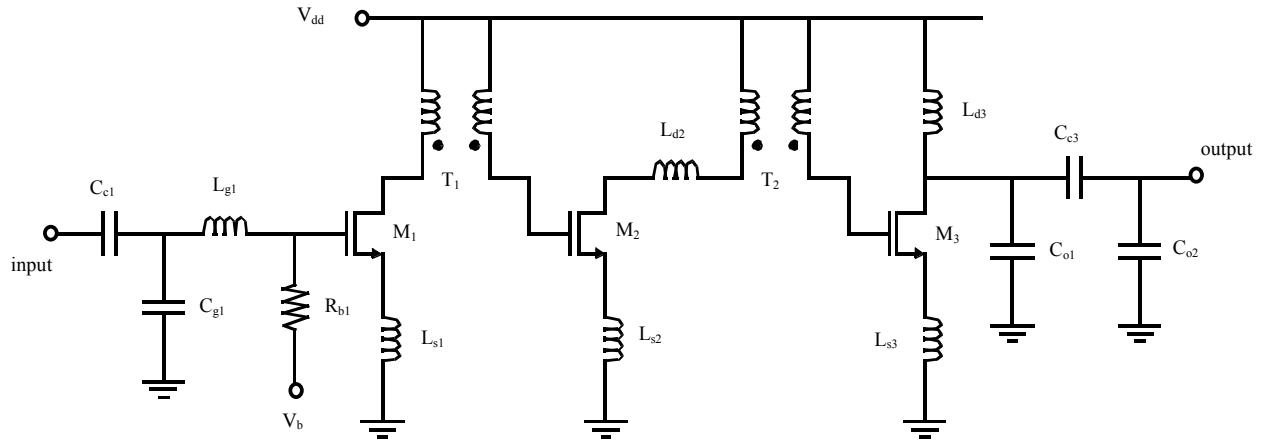


Fig. 2 Schematic of the 77GHz single-ended low noise amplifier

The corresponding drain current density is 0.31 mA/ $\mu$ m.

The input matching network is formed by inductor  $L_{g1}$  (175pH) and capacitors  $C_{g1}$  (25fF) and  $C_{c1}$  (200fF) as an L-match.  $C_{c1}$  concurrently acts as a DC block capacitor.  $C_{g1}$  is realized by using the parasitic capacitances of  $L_{g1}$  and  $C_{c1}$ .  $M_1$ 's gate terminal is biased via resistor  $R_{b1}$ .

The second and third stages are optimized for maximum gain and stability. They consist of transistors  $M_2$  and  $M_3$  with degeneration inductor  $L_{s2}$  and  $L_{s3}$ , respectively. Transistors  $M_{2,3}$  are identical with 20 fingers of 1 $\mu$ m wide gates. Both  $L_{s2}$  and  $L_{s3}$  have value of 100pH. The noises from the second and third stages are suppressed by the first stage's power gain. Thus,  $M_2$  and  $M_3$  gate bias voltages are set at 1V for maximum drain current density and maximum power gain instead of minimum noise figure.

Inductive degeneration of the second and third stage, as a local negative feedback network around  $M_2$  and  $M_3$ , respectively, improves the overall linearity and stability. Unconditional stability is desired to avoid parasitic oscillation due to signal feedback from the finite supply or ground bondwires inductance or poor signal isolation from the conductive silicon substrate.

The first and second stages are conjugate matched to maximize the power transfer between stages. They are coupled by an on-chip resonant tuned transformer  $T_1$ .  $T_1$  also act as inter-stage matching network [7].  $T_1$  transforms the capacitive gate impedance of  $M_2$  to an inductive impedance at the drain of  $M_1$ . Similarly, transformer  $T_2$  and inductor  $L_{d2}$  provide conjugate matching between output of the second stage  $M_2$  and input of the third stage  $M_3$ . Transformers  $T_1$  and  $T_2$  are implemented with a pairs of interwound single-turn coil using the top metal layer. The self-inductance of each coil for  $T_1$  and  $T_2$  are 82pH and 73pH, respectively. The magnetic coupling factor for both transformer are 0.4. Inductor  $L_{d2}$ , with a value of 130pH, introduces an extra phase shift in the primary port of  $T_2$ . The gate and drain voltages of transistors  $M_2$  and  $M_3$  are biased through the transformers  $T_1$  and  $T_2$  at 1V.

The LNA output is matched to 50 $\Omega$  for measurement purpose. In practice, the third stage  $M_3$  will drive the input port of the receive mixer. Thus output matching network should maximize the power transfer between the LNA output port and the mixer input port. In the current setup, output matching network is formed by inductor  $L_{d3}$  (100pH) and capacitors  $C_{o1}$ ,  $C_{o2}$  and  $C_{c3}$  as a  $\pi$ -match.  $C_{c3}$  concurrently acts as a DC block capacitor.  $C_{o1}$ , with a value of 15fF, is the sum of the parasitic capacitances of  $L_{d3}$ ,  $C_{c3}$  and drain diffusion capacitance of  $M_3$ .  $C_{o2}$ , with a value of 10fF, is the bottom-plane parasitic capacitance of  $C_{c3}$ .  $C_{c3}$  is a metal-insulator-metal (MIM) capacitor with a value of 30fF.

### III. SIMULATION RESULTS

#### A. 2-Port S-parameters

The LNA performance characterization is measured by the 2-port S-parameters. The  $S_{11}$  and  $S_{22}$  measured the amplifier's input and output return losses, respectively. The amplifier power gain is measured by the  $S_{21}$  parameter while the reverse isolation is measured by the  $S_{12}$  parameter. The simulated full 2-port S-parameters are shown in Fig. 3 for frequency range between 40 and 120GHz.

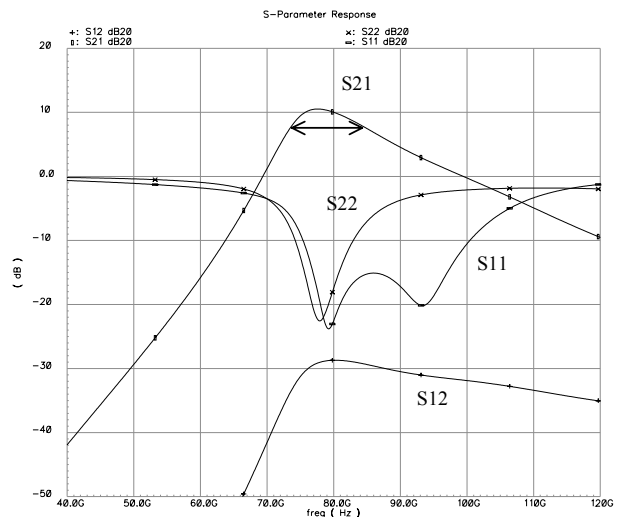


Fig. 3 Simulated 2-port S-parameters

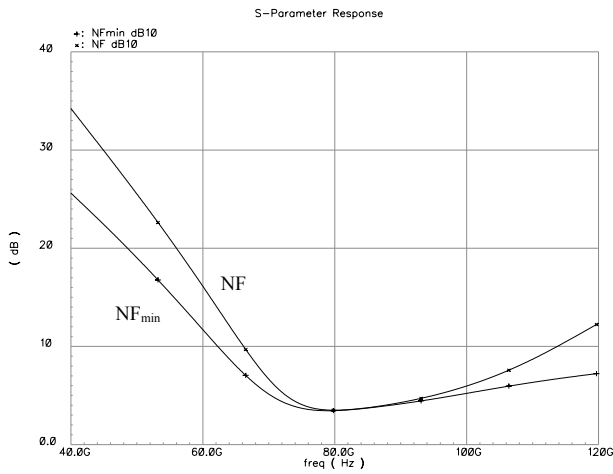


Fig. 4 Simulated noise figure and minimum noise figure

Simulation predicts the LNA featuring a bandpass response and having an overall power gain of 10.5dB at 77GHz. The -3dB power gain frequency is from 74.3 to 82.8GHz and equivalently giving a -3dB bandwidth of 8.5GHz, centered at 79GHz.

Both the input and output ports are matched to 50Ω. The frequency ranges where the input and output return loss are less than -10dB are from 75.4 to 100.4GHz and from 74.2 to 82.9GHz, respectively. The overlapping region is from 75.4 to 82.9GHz. This gives an effectively return loss bandwidth of 7.5GHz centered at 79GHz.

The input is wideband matched with a -10dB bandwidth of 25GHz. The bandwidth of the output matching is of less important because it is only for measurement purpose.

The LNA reverse isolation is better than -28.7dB across 40 to 120GHz. This ensures good isolation between the amplifier's input and output ports, avoiding potential instability and parasitic oscillation.

### B. Noise Figure

As the first stage of the receiver chain, the LNA should have as low noise figure as possible since it has the dominant effect on the noise performance of the whole system. A low noise figure of the LNA will enhance the receiver's sensitivity.

The LNA noise performance is captured by the 50Ω noise figure ( $NF_{50}$  or simply NF) and the minimum noise figure ( $NF_{min}$ ). NF is the device noise figure when measured with 50Ω source impedance. On the other hand,  $NF_{min}$  is the measured noise figure with optimum source impedance and it is the absolute minimum noise figure available from the amplifier. If NF and  $NF_{min}$  coincidence with each other, the LNA is said to have the optimum noise performance.  $NF_{min}$  could be measured by an impedance tuner where the source impedance varies until a minimum noise figure is found across a specified frequency range.

The simulated noise figure and minimum noise figure of the LNA are shown in Fig. 4. At 80GHz, the noise figure has a

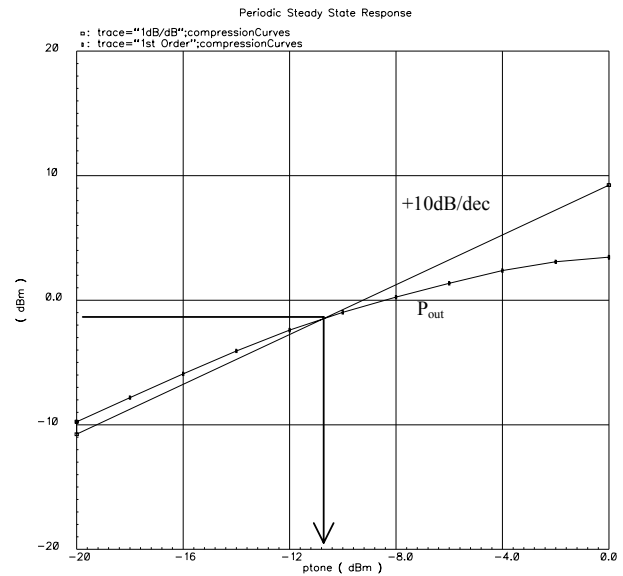


Fig. 5 Simulated input -1dB compression point

minimum value of 3.5dB. It has a value of 3.6dB at 77GHz. On the other hand, the minimum noise figure has a value of 3.5dB at 80GHz. Thus, the proposed LNA gives optimum noise performance around 80GHz. From 76 to 90GHz, NF and  $NF_{min}$  are closed and almost being identical. From 75-87GHz, with a bandwidth of 12GHz, the noise figure is less than 4dB.

### C. Linearity

Amplifier's linearity is characterized by the -1dB compression ( $P_{-1dB, in}$ ) and the third-order intercept point ( $IP_3$ ). Fig. 5 shows the single-tone compression characteristic. A 77GHz sinusoidal is applied at the LNA input port with power range from -20 to 0 dBm. As seen, the input -1dB compression is -10.8dBm.

Another measure of amplifier's linearity is  $IP_3$ . Two sinusoidal tones at 76.5 and 77.5GHz, both having power of -20dBm, are applied to the LNA input port. The LNA output spectrum is shown in Fig. 6. Two sidebands at 75.5 and 78.5GHz are generated by the LNA non-linear characteristic. The input  $IP_3$  is calculated to be -1.5dBm.

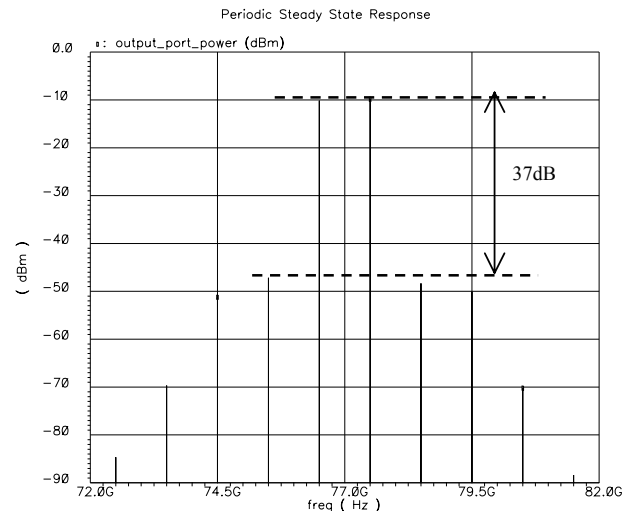


Fig. 6 Simulated output frequency spectrum for 2-tones input

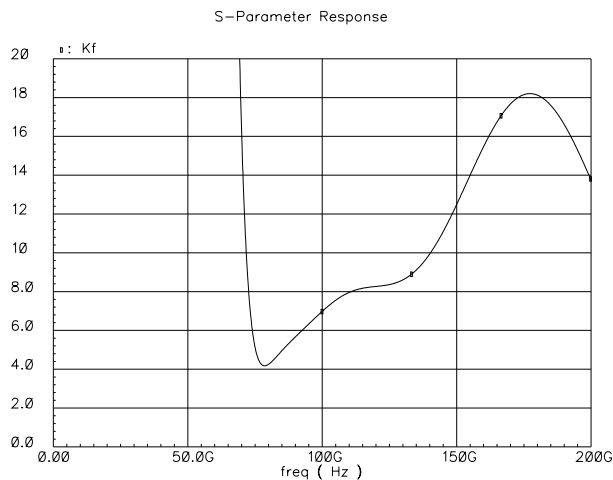


Fig. 7 Simulated stability factor (K)

#### D. Stability

Unconditional stability is desired to avoid parasitic oscillation. The stability characteristic of an amplifier is measured by the K. Fig. 7 shows the simulated K from 100MHz to 200GHz. K is larger than 4 for all frequency range, indicating the amplifier is unconditional stable.

#### E. DC Performance and summary

Low power device extend the battery lifetime for portable consumer applications. The power dissipation of the presented LNA is 18.5mW, for a supply voltage of 1V. Table 1 summarized the LNA performance.

### IV. CONCLUSION

A 77GHz LNA is designed in a 90nm CMOS process. A three stages implementation gives an overall power gain of 10.5dB. The input and output impedance match to 50Ω and have a return loss less than -10dB and pass bandwidth of 7.5GHz at 79GHz. Noise figure reaches the device minimum noise figure at 80GHz with value of 3.5dB. From 75 to 87GHz, the noise figure is less than 4dB. The input IP3 is -1.5dBm with two frequency tones applied at 76.5GHz and 77.5GHz. The -1dB compression point is -10.8dBm for a supply voltage of 1V and current consumption of 18.5mA. The stability factor (K) is larger than 4 and  $\Delta$  is smaller than 1 from 100MHz to 200GHz, showing that the amplifier is unconditional stable.

Table 1 Performance summary

Power Gain	10.5dB
Noise Figure	3.5dB
$P_{-1dB, in}$	-10.8dBm
IIP3	-1.5dBm
-3dB bandwidth	8.5GHz
Supply Voltage	1V
Power Consumption	18.5mW
Technology	90nm CMOS

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