

Comparing DLLs and Shift Registers for Low-Jitter Multi-phase Clock Generation

Xiang Gao, Eric A.M. Klumperink, Bram Nauta

Abstract—In this paper we compare a Shift Register (SR) to a Delay Locked Loop (DLL) for Multi Phase Clock Generation (MPCG), and motivate why a SR is often better. For a given power budget, we show that a SR generates less jitter than a DLL when both are realized with Current Mode Logic (CML) circuits and white noise is assumed. This is due to differences in jitter accumulation and the possibility to choose latch delays in a SR much smaller than the delays of DLL elements. For N -phase clock generation, the SR also functions as a divide-by- N and requires a VCO with N times higher frequency than the DLL counterpart. However, this can be done in a power neutral way and can even have advantages like higher quality factor and less area for the inductors.

Index Terms—Multi-phase Clocks, Current Mode Logic, Delay Locked Loop, Jitter, Shift Registers.

I. INTRODUCTION

MULTI phase clocks are useful in many applications. In high-speed serial link applications [1], multi-phase clocks are used to process data streams at a bit rate higher than the internal clock frequencies and in time-interleaved ADCs [2] to achieve high ADC sampling rates while keep the resolution high. In wideband wireless communication systems, harmonic rejection mixers and multi-path poly-phase circuits driven by multi-phase clocks are used to reject unwanted harmonics and sidebands [3].

For multi-phase clock generation, delay-locked loops (DLLs) are often used. Other than a DLL, a shift register can also be used to generate multi-phase clocks [3]. Compared with a DLL multi-phase clock generator (MPCG), a shift register based MPCG uses N times higher frequency for N -phase clock generation and at first glance seems to have more power consumption. However, there is no jitter accumulation from one clock phase to the other in a shift register as in a DLL, which should be taken into account for a fair comparison [4]. This work makes a solid comparison between MPCGs using a DLL and a shift register, primarily based on their power and jitter performance.

The rest of the paper is arranged as follows. Section II describes the architecture of a DLL MPCG and analyses its jitter performance, while section III addresses the SR. These

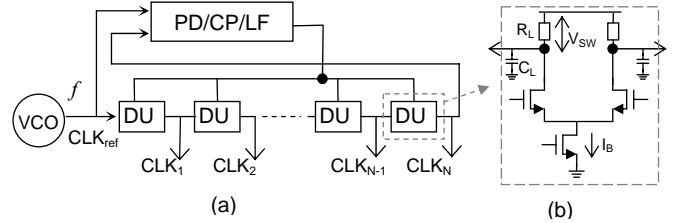


Fig. 1. (a) DLL MPCG architecture (b) CML delay unit schematic

two structures are then compared in Section IV. In section V, the simulation results are presented and Section VI discusses the conclusions.

II. DLL MPCG JITTER

A. DLL MPCG Architecture

The architecture of a DLL based MPCG is shown in Fig. 1(a). It consists of a voltage controlled delay line (VCDL) which has N identical delay units (DUs) and a control loop which is formed by a phase detector (PD), a charge pump (CP) and a loop filter (LF). In the DLL, a reference clock generated by a VCO, CLK_{ref} , with the wanted frequency f is propagated through the VCDL. The loop compares the phase of the last output of the VCDL CLK_N with CLK_{ref} and controls the VCDL so that the total delay time is one reference clock period. Therefore, the outputs of the N DUs $CLK_1 \sim CLK_N$ are multi-phase clocks with ideally $2\pi/N$ phase shift in between.

B. DLL MPCG Output Jitter

In this work, we assume all noise sources are white and analyze absolute jitter performance, for simplicity.

The DLL MPCG output jitter can be divided into three parts: 1) jitter transferred from the reference clock, 2) jitter generated by the VCDL and 3) jitter from the control loop. For an optimal DLL design, the jitter contribution of the control loop is negligible [5] and thus ignored hereafter.

When the reference clock jitter is transferred to the DLL outputs, it has been shown in [5][6] that jitter peaking always exists. The DLL cannot decrease reference clock jitter, but jitter peaking can be very small by choosing a low DLL loop bandwidth.

For jitter generated by the VCDL, it has been shown in [5][6] that the DLL renders no improvement. Again, the VCDL noise jitter is lowest for low values of the loop bandwidth, in which case it would be almost equal to that of a free-running VCDL [5]. The jitter will thus accumulate from

Manuscript received September 24, 2007.

The authors are with the IC-Design Group, CTIT, University of Twente, 7500 AE, Enschede, The Netherlands (e-mail: X.Gao@utwente.nl).

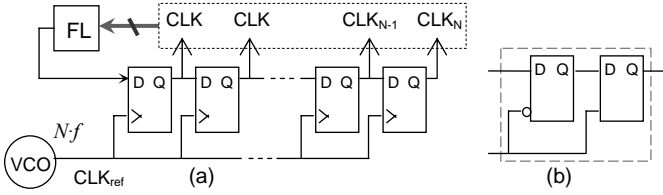


Fig. 2. (a) SR MPCG architecture (b) DFF block schematic

one delay unit to the other. If the jitter variance of one delay unit is $\sigma_{i,DU}^2$, the jitter variance on the output of the n^{th} delay unit will be n times bigger. For multi-phase clock applications like the software defined radio transmitter [3], the jitter of every clock phase is equally relevant. To measure the jitter performance of the N -phase clocks, average jitter variance is used, which can be calculated as:

$$(\sigma_{i,DLL}^2)_{\text{avg}N} = \frac{1}{N} \cdot \sum_{n=1}^N (n \cdot \sigma_{i,DU}^2) = \frac{N+1}{2} \sigma_{i,DU}^2 \quad (1)$$

III. SR MPCG JITTER

A. SR MPCG Architecture

The architecture of a SR MPCG is shown in Fig. 2(a). It consists of a D flip-flop (DFF) chain with N identical DFFs. A reference clock CLK_{ref} , generated by a VCO with a frequency of Nf , is fed into the DFF chain. A flip logic (FL) circuit monitors the N outputs of the DFF chain and flips the logic value at the D input of the first DFF twice every N reference clock cycles. In other words, the outputs of the DFF chain run at a frequency of f and the SR based MPCG also functions as a divide-by- N divider. Since a DFF is sensitive to rising edges, the Q output of each DFF is delayed from the previous DFF's output by one reference clock period, which is equivalently a $2\pi/N$ phase delay. In this way, N -phase clocks $CLK_1 \sim CLK_N$ are generated.

B. SR MPCG Output Jitter

The SR MPCG output jitter can be divided into two parts: jitter transferred from the reference clock and jitter generated by the DFF chain. The flip logic is simply a logical “enabler” for the first DFF and will not contribute to jitter. In an example of 12-phase clock generation in [3], the flip logic was implemented with a simple NOR gate with CLK_6 and CLK_{12} as its inputs.

For the jitter transferred from the reference clock, the SR MPCG renders no improvement. Any timing error at the reference clock will be transferred to the DFF chain outputs.

In Fig.2(a), the output jitter of a DFF is not affected by the jitter of the previous DFF since the previous DFF only acts as an “enabler” while the VCO defines the timing. Therefore, there is no jitter accumulation from one clock phase to the other clock phase as in the DLL MPCG. A DFF can be designed with two master/slave latches as shown in Fig. 2(b). For a proper design, only the second latch contributes to jitter since the first is just an “enabler”. If we define the rms jitter

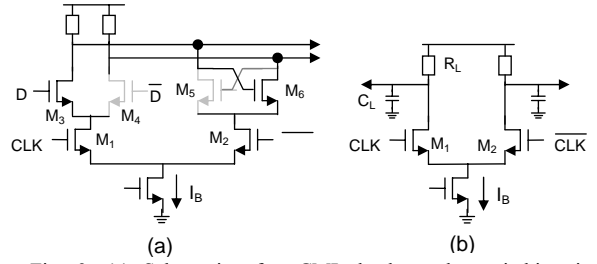


Fig. 3. (a) Schematic of a CML latch at the switching instant. (b) Simplified schematic for jitter analysis.

variance of one latch as $\sigma_{i,Latch}^2$, the average jitter variance for the set of N -phase clocks generated by the SR can be easily calculated as:

$$(\sigma_{i,SR}^2)_{\text{avg}N} = \sigma_{i,Latch}^2 \quad (2)$$

IV. COMPARISON BETWEEN DLL AND SR JITTER

A. Comparing Jitter Transferred from Reference Clock

From the above analysis, we see that the DLL and SR MPCGs both render no improvement on the reference clock jitter. However, the SR MPCG requires a reference clock with N times higher frequency than that of the DLL equivalent. If the reference clock is generated by a VCO¹, the VCO for the SR should work at N times higher frequency. This may lead to the concern that the SR puts more requirements on the VCO.

Assuming the VCO has an f^{-2} power spectrum and its quality of design is adequately assessed via the often used figure of merit FOM [7], the single sideband phase noise to carrier ratio at an offset frequency f_m can be expressed as:

$$L(f_m) = \frac{10^{FOM/10}}{P_{VCO}} \cdot \frac{f_{VCO}^2}{f_m^2} \quad (3)$$

where f_{VCO} is the frequency and P_{VCO} is the power dissipation in [mW]. It is well-known that the variance for stationary absolute jitter is related to the total area of its power spectrum, i.e. the reference clock jitter variance $\sigma_{i,ref}^2$ becomes:

$$\sigma_{i,ref}^2 = \frac{2 \times \int_{f_l}^{f_h} L(f_m) df_m}{(2\pi f_{VCO})^2} = \frac{10^{FOM/10}}{2\pi^2 \cdot P_{VCO}} \cdot \left(\frac{1}{f_l} - \frac{1}{f_h} \right) \quad (4)$$

where $[f_l, f_h]$ is the specified integration region. Equation (4) indicates that although the VCO in the SR MPCG runs at N times higher frequency, it outputs the same jitter, given the same power and the same quality of design. If an LC VCO is used, higher working frequency may even be preferred, since the quality factor of an inductor ($\omega L/R$) increases with frequency and smaller inductors are needed (less chip area).

¹ If the VCO is part of a synthesizer, the synthesizer for the SR MPCG may need an extra divide-by- N . However, this is not necessary since the SR MPCG itself functions as a divide-by- N and can be re-used.

B. Comparing Jitter Generated by VCDL and DFF Chain

Because of better supply noise rejection, current mode logic (CML) circuits are often used in low jitter designs. To compare the jitter generated by the two MPCGs, we assume that they both use CML circuits. The simplified schematic of a CML delay unit is shown in Fig. 1(b). It is based on an NMOS source coupled differential pair driving the resistive load R_L and biased by a current source I_B . As the loads are RC circuits, the propagation delay t_d can be approximated as:

$$t_d = \ln 2 \cdot R_L C_L = \ln 2 \cdot (V_{SW} / I_B) \cdot C_L \quad (5)$$

where V_{SW} is the differential output swing and is determined by R_L and I_B due to the full switching of the tail current.

The CML implementation of a latch is shown in Fig. 3(a). For a proper operation, the D inputs of the latch should be already stable before the CLK starts to switch. For example, D is high and \bar{D} is low and therefore, at the switching moment, transistors M4 and M5 are off. M3 and M6 are in their saturation region and work as cascode transistors on top of the differential pair. The noise contribution of M3-M6 can thus be neglected. The schematic of the latch can be simplified to Fig. 3(b) which is exactly the same as the schematic of the CML delay unit in Fig. 1(b). Therefore, we can apply the same noise jitter analysis for the delay unit and the latch.

The jitter variance of the circuit shown in Fig.3(b) can be predicted using the analysis presented in [8] as:

$$\sigma_i^2 = (1 + \gamma + \gamma_T) \cdot \frac{g_{mT} R_L}{2} \cdot \frac{2kTC_L}{I_B^2} \quad (6)$$

where γ and γ_T are respectively the noise factor of the transistors of the differential pair and the tail bias transistor. g_{mT} is the transconductance of the tail bias transistor. This transconductance can also be represented by the bias current I_B and overdrive voltage $V_{OV,T}$ of the tail bias transistor:

$$g_{mT} = \alpha \frac{I_B}{V_{OV,T}} \quad (7)$$

with α the transistor model parameter which is equal to two for the square-law model. With (5) and (7), (6) can be rewritten as:

$$\sigma_i^2 = (1 + \gamma + \gamma_T) \cdot \frac{\alpha I_B R_L}{2V_{OV,T}} \cdot \frac{2kTC_L}{I_B^2} = (1 + \gamma + \gamma_T) \cdot \frac{\alpha V_{SW}}{2V_{OV,T}} \cdot \frac{2kTC_L}{I_B^2} \quad (8)$$

In most of the clock generator designs, jitter and power are two important parameters. Via admittance level scaling [9], noise power and hence jitter variance can always be reduced at the cost of increasing the power consumption P . In order to take this tradeoff into account and make a fair comparison, jitter variance is normalized to power, with 1mW as reference:

$$(\sigma_i^2)_{NorP} = \sigma_i^2 \cdot (P / 1mW) \quad (9)$$

For the same circuit, applying admittance level scaling will not change the value of its $(\sigma_i^2)_{NorP}$. A design with a smaller $(\sigma_i^2)_{NorP}$ means it generates less jitter, given the same amount

of power. For a CML circuit, the power consumption is dominated by the static power $I_B \cdot V_{DD}$. With (8) and (9), for both the CML delay unit and latch we find:

$$(\sigma_i^2)_{NorP} = (1 + \gamma + \gamma_T) \cdot \frac{\alpha V_{SW}}{2V_{OV,T}} \cdot \frac{2kT \cdot V_{DD}}{1mW} \cdot \frac{C_L}{I_B} \quad (10)$$

Substituting (5) into (10) yields:

$$(\sigma_{i,noise}^2)_{NorP} = \left\{ (1 + \gamma + \gamma_T) \cdot \frac{\alpha V_{SW}}{2V_{OV,T}} \cdot \frac{2kT \cdot V_{DD}}{\ln 2 V_{SW} \cdot 1mW} \right\} \times t_d \quad (11)$$

Equation (11) indicates that the normalized noise jitter variance is proportional to t_d for a given power budget.

In a DLL, if t_d is tuned by tuning R_L while keep V_{SW} constant, I_B thus $V_{OV,T}$ in (11) will vary with t_d . This second order effect will be discussed in Section V. Here to simplify the comparison, we ignore this effect and assume the delay unit and the latch have the same V_{SW} and $V_{OV,T}$. A DLL has N delay units contributing to jitter and power while a SR has N latches contributing to jitter and $2N$ latches dissipating power. The average noise jitter variance generated by the DLL and the SR MPCGs can then be compared with (1), (2) and (11), as:

$$\frac{(\sigma_{i,SR}^2)_{avgN,NorP}}{(\sigma_{i,DLL}^2)_{avgN,NorP}} = \frac{(\sigma_{i,Latch}^2)_{NorP} \times 2N}{\frac{N+1}{2} \times (\sigma_{i,DU}^2)_{NorP} \times N} = \frac{4}{N+1} \cdot \frac{t_{d,Latch}}{t_{d,DU}} \quad (12)$$

The comparison result thus depends on the amount of delay of the delay unit $t_{d,DU}$ and that of the latch $t_{d,Latch}$. In a DLL MPCG, the VCO defines the frequency and the VCDL defines the delay in between the N output clocks. Both the VCO and the delay line need to be tuned for the MPCG to generate N -phase clocks at different frequency f . The delay of one delay unit is functionally required to be the output clock period T divided by N :

$$t_{d,DU} = \frac{T}{N} = \frac{1}{N \cdot f} \quad (13)$$

In contrast, the SR MPCG is more flexible. For different f , only the VCO needs to be tuned since both the frequency and the delay in between the N output clocks are defined by the VCO. The only concern is that the DFFs should operate correctly, which requires [10]:

$$t_{d,Latch} + t_{su} \leq \frac{1}{N \cdot f} \quad (14)$$

where t_{su} is the setup time required by the DFF. Defining the maximum working frequency of a SR MPCG for N -phase clock generation in a certain technology as $f_{max,SR}$, the latch delay will have its minimum value $t_{d,Latch,min}$ at $f_{max,SR}$ as:

$$t_{d,Latch,min} = \frac{1}{1+a} \cdot \frac{1}{N \cdot f_{max,SR}} \quad (15)$$

with a the ratio between $t_{d,Latch,min}$ and t_{su} .

Since a small delay is preferred for a small $(\sigma_{i,noise}^2)_{NorP}$, the latch delay can be flexibly chosen to its minimum value as in

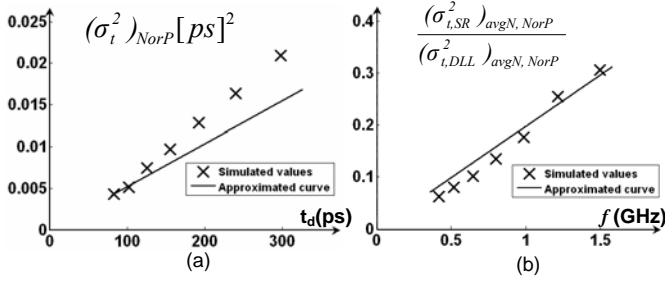


Fig. 4. Noise jitter simulation results in 0.13 μ m CMOS with $N=8$ for (a) a CML delay unit (b) DLL and SR comparison.

(15). For a delay unit, the delay is limited by (13). Taking this factor into account, (12) can be re-written as:

$$\frac{(\sigma_{t,SR}^2)_{avgN,NorP}}{(\sigma_{t,DLL}^2)_{avgN,NorP}} = \frac{1}{1+a} \cdot \frac{f}{f_{max,SR}} \cdot \frac{4}{N+1} \quad (16)$$

As soon as the wanted number of clock phases is larger than three ($N>3$), (16) is smaller than one since the DFF needs a finite setup time ($a>0$) and the working frequency of the SR can't surpass the technology limit ($f \leq f_{max,SR}$). This means that the SR based MPCG generates less noise jitter than the DLL counterpart for a given power budget. Equation (16) also indicates that the advantage of the SR based MPCG will be larger if more advanced technologies are used and in applications where clocks with larger number of phases at lower frequencies are needed.

V. SIMULATION RESULTS

In order to verify the calculations, simulations were done for a DLL and a SR for $N=8$ in 0.13- μ m CMOS. The reference clocks are voltage sources with 1Kohm source resistance. The VCDL delay is tuned by tuning the load resistance as suggested by (22) while keep V_{SW} to be 0.6V. For the DFFs, a is about 0.5. The load capacitance is 100fF, which is comparable to the parasitic capacitances. In this implementation, $f_{max,SR}$ is about 1.5 GHz. Fig.4 shows the jitter simulation results using strobed PNoise analysis in Spectre. The simulated values fit the predicted curve. The deviation when t_d is high is expected by (12) since I_B and thus $V_{OV,T}$ is lower for a higher t_d . The jitter is then higher.

VI. CONCLUSION

Analysis show that, for a given power budget, a shift register based MPCG generates less jitter than a DLL equivalent when both are realized with current mode logic circuits. This is partly because a SR MPCG has no jitter accumulation from one clock phase to the other as in a DLL MPCG. In addition, a SR can use latches with very small delay time, while jitter generation of a CML circuit is proportional to its (functionally required) delay time. Although a SR MPCG requires a reference clock with higher frequency, it does not lead to additional power consumption on the VCO. The advantage of a SR MPCG will be larger as technology advances and in

applications where clocks with larger number of phases at lower frequencies are needed.

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