

Optimisation of Programmable Operational Amplifiers

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Abstract— An optimisation of a programmable Operational Amplifier is presented. The OpAmp is programmable concerning noise and power consumption while keeping the stability for the whole range of programmability. Simulation results for a 0.35 μm CMOS OpAmp show either low noise of 3.2 nV/ $\sqrt{\text{Hz}}$ or low power consumption of 84 μW having a phase margin variation of only $\Delta\phi_{\text{res}} = 3^\circ$.

Keywords— low noise OpAmp; low power OpAmp; programmable OpAmp

I. INTRODUCTION

In comparison to conventional Operational Amplifiers, programmable OpAmps have the advantage of being adaptable to the given circuit specification. This allows the design of multi-purpose microchips [1]. The fabrication of higher quantities is hence feasible, leading to lower production costs. While programmable OpAmps are quite known in general [2,3], only few materials can be found on their design methodology.

In [4] a methodology for the systematic design of a programmable OpAmp was presented. The adopted rail-to-rail folded-cascode OpAmp is based on [5-7]. Its architecture only allows a phase margin dependent on the current consumption, which leads to an over- or under-compensation of the OpAmp if the current consumption is changed. Experimental results showed a phase margin varying from 74° down to 16° where the power consumption is increased from 140 μW to 30 mW reducing the input noise from 14 nV/ $\sqrt{\text{Hz}}$ down to 2 nV/ $\sqrt{\text{Hz}}$ [4]. In this paper an improved OpAmp architecture is proposed, which ensures a nearly constant phase margin over the whole range of programmability. Section II describes the architecture of the programmable OpAmp and its theoretical model, while Section III highlights the simulation results. In Section IV conclusions are given.

II. ARCHITECTURE

The improved architecture of the programmable Operational Amplifier is shown in figure 1. The key

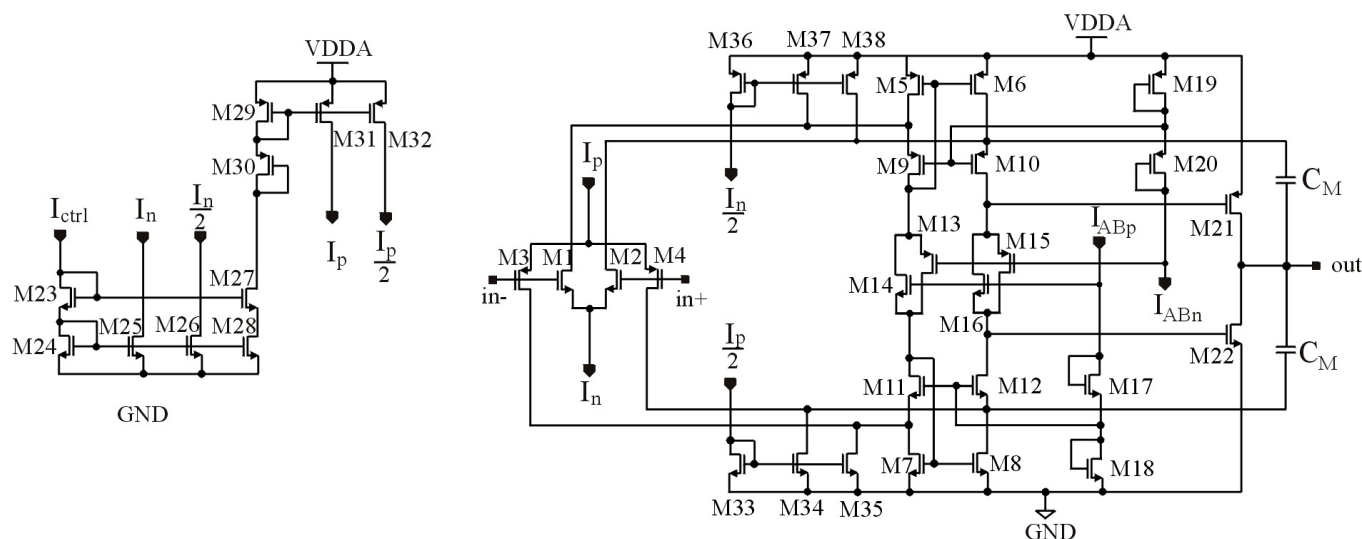


Figure 1: Schematic of the improved OpAmp architecture.

problem of having phase margin variation over the operation range [4] is simply solved by using two additional current mirrors $M_{33} - M_{38}$. In the following it is shown how these additional current mirrors influence the current dependence of the OpAmp.

The transfer characteristics of the given OpAmp architecture can be described as

$$A(\omega) = \frac{A_0}{1 + \frac{s}{\omega_d}} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right) \left(1 - \frac{s}{\omega_z}\right)}{1 + \frac{\sqrt{2Q^2 - 1}}{\sqrt{2Q^2}} \cdot \frac{s}{\omega_{nd}} + \frac{2Q^2 - 1}{2Q^2} \frac{s^2}{\omega_{nd}^2}}, \quad (1)$$

where ω_d and ω_{nd} are the frequencies of the dominant and nondominant pole, respectively, ω_z are the zeros and A_0 is the overall dc gain. Q denotes the quality factor with $Q > 1/\sqrt{2}$ and describes the *Gain Peaking* A_{peak} at ω_{nd} [8,9] with

$$A_{peak} = \frac{2Q^2}{\sqrt{4Q^2 - 1}}. \quad (2)$$

The frequencies ω_{nd} , ω_z and the quality factor Q are given by

$$\omega_{nd} = \sqrt{\frac{2g_{m12}g_{m22}}{C_L C_{gs22}} \left(1 - \frac{1}{2Q^2}\right)}, \quad (3)$$

$$\omega_z = \sqrt{\frac{g_{m12}g_{m22}}{C_M C_{gs12}}}, \quad (4)$$

$$Q = \sqrt{\frac{g_{m22}C_L}{2g_{m12}C_{gs22}} \frac{2C_M}{2C_M + C_L}}. \quad (5)$$

Choosing $\omega_z \geq 2\omega_{nd}$, the zeros can be neglected in first order and eq. (1) becomes with $s = j\omega$

$$A(\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_d}} \cdot \frac{1}{1 + \frac{\sqrt{2Q^2 - 1}}{\sqrt{2Q^2}} \cdot \frac{j\omega}{\omega_{nd}} - \frac{2Q^2 - 1}{2Q^2} \frac{\omega^2}{\omega_{nd}^2}}. \quad (6)$$

In [4] the two constraints

$$I_{D12} = d \cdot I_{D1}^2 \quad (7)$$

$$\text{and } I_{D22} = e \cdot I_{D1}^2 \quad (8)$$

were introduced to achieve an independence of the Miller capacitance C_M of any bias current. An increase of current consumption to minimize noise then has no influence on the stability of the operational amplifier. If a phase margin of $\varphi_{res} = 70^\circ$ and a gain at ω_{nd} of $|A(\omega_{nd})| < 1$ for the whole operation range is defined, the Miller capacitance and the W/L ratio of transistor M_{12} become [4]

$$C_M \approx \frac{A_x Q^2 k C_{gs22}}{2\sqrt{(2Q^2 - 1)K'_n \frac{W_{22}}{L_{22}} e}} \left(1 + \sqrt{1 + \frac{2\sqrt{(2Q^2 - 1)K'_n \frac{W_{22}}{L_{22}} e C_L}}{A_x Q^2 k C_{gs22}}}\right) \quad (9)$$

$$\text{and } \frac{W_{12}}{L_{12}} = \frac{4C_L^2 C_M^4 e}{C_{gs22}^2 (C_L + 2C_M)^4 Q^4 d} \frac{W_{22}}{L_{22}}, \quad (10)$$

where A_x is

$$A_x = \frac{\sqrt{4Q^2 - 2}}{4Q^2 \tan 20^\circ} \left(1 + \sqrt{1 + (2Q \tan 20^\circ)^2}\right) \quad (11)$$

The input transistors $M_1 - M_4$ are in subthreshold region to achieve minimal input noise. All other transistors are driven in saturation. The quality factor Q is set to 1.5 [4]. The factor k is between 27 1/V and 30 1/V [10]. Hence, eqs. (9) and (10) show the independency of the Miller capacitance C_M and the W/L ratio of transistor M_{12} of any current.

With $I_{D1} = I_{D3}$, $I_{D13} = I_{D14}$ (electrical symmetry) and $I_{D7} = I_{D8}$ (current mirror), from the translinear loop M_7 , M_{14} , M_{17} and M_{18} the relationship

$$I_{D17} \approx \frac{1}{4} \cdot \frac{W_{17}}{L_{17}} \left(\sqrt{\frac{L_7}{W_7}} + \sqrt{\frac{1}{2} \cdot \frac{L_{14}}{W_{14}}}\right)^2 I_{D12} \quad (12)$$

is obtained. Further, with $V_{gs7} \approx V_{gs22}$ the current flowing through M_{22} is determined by

$$I_{D22} \approx \frac{W_{22}}{L_{22}} \cdot \frac{L_7}{W_7} I_{D12}. \quad (13)$$

Inserting eq. (7) into (12) and (13), quadratic relationships of I_{D17} and I_{D22} to I_{D1} are obtained

$$I_{D17} = g \cdot I_{D1}^2 \quad (14)$$

$$I_{D22} \approx \frac{W_{22}}{L_{22}} \cdot \frac{L_7}{W_7} d I_{D1}^2, \quad (15)$$

where g is

$$g \approx \frac{1}{4} \cdot \frac{W_{17}}{L_{17}} \left(\sqrt{\frac{L_7}{W_7}} + \sqrt{\frac{1}{2} \cdot \frac{L_{14}}{W_{14}}}\right)^2 d. \quad (16)$$

Equation (15) shows that in contrast to [4] eq. (8) is now exactly satisfied, which is due to the new current mirrors $M_{33} - M_{38}$. Hence, the OpAmp remains stable with a constant phase margin of $\varphi_{res} = 70^\circ$ over the whole range of programmability.

Using (8) in (15), factor e is calculated to

$$e \approx \frac{W_{22}}{L_{22}} \cdot \frac{L_7}{W_7} d. \quad (17)$$

The W/L ratio of transistor M_{14} is calculated from (16) to

$$\frac{W_{14}}{L_{14}} \approx \frac{1}{2 \cdot \left(\sqrt{4 \cdot \frac{g}{d} \cdot \frac{L_{17}}{W_{17}}} - \sqrt{\frac{L_7}{W_7}} \right)^2}. \quad (18)$$

The ratio W_7/L_7 is determined from the input noise specification e_{nOP}^2 . The overall noise of the OpAmp is calculated to [11]

$$e_{nOP}^2 = \left(1 + \frac{g_{m7}}{g_{m1}} \right) \frac{8k_B T}{3kI_{D1}}. \quad (19)$$

Using $z = g_{m7}/g_{m1}$, the W/L ratio of transistor M_7 and I_{D1} become

$$\frac{W_7}{L_7} = \frac{z^2 k^2}{2K'_n d} \quad (20)$$

$$\text{and } I_{D1} = \frac{8k_B T(z+1)}{3ke_{nOP}^2}. \quad (21)$$

A minimal and maximal current $I_{D1,min}$ and $I_{D1,max}$ of transistor M_1 is defined by the maximum and minimum input noise $e_{nOP,max}$ and $e_{nOP,min}$, respectively. With (17), (20) and $C_{gs} = 2/3WLC'_{ox}$, eqs. (9) and (10) become

$$C_M \approx \frac{A_x Q^2 k^2 z L_{22}^2 C'_{ox}}{3K'_n d \sqrt{(4Q^2 - 2)}} \left(1 + \sqrt{1 + \frac{3K'_n d \sqrt{(4Q^2 - 2)} C_L}{A_x Q^2 k^2 z L_{22}^2 C'_{ox}}} \right) \quad (22)$$

$$\text{and } \frac{W_{12}}{L_{12}} = \frac{18K'_n C_L^2 C_M^4 d}{z^2 k^2 L_{22}^4 C'_{ox} (C_L + 2C_M)^4 Q^4}. \quad (23)$$

The W/L ratio of transistor M_{22} is calculated with the help of the constraint for the zeros $\omega_c \geq 2\omega_{nd}$ which yields

$$\frac{W_{22}}{L_{22}} \geq \frac{8C_M}{C_L} \frac{W_{12} L_{12}}{L_{22}^2} \left(1 - \frac{1}{2Q^2} \right). \quad (24)$$

The specified W/L -ratios of the transistors given in (18), (20), (23), (24) and the Miller capacitance C_M from eq. (21) are only dependent on W_{17}/L_{17} , d , g , z and C_L . The parameters W_{17}/L_{17} , d , g and z are determined by an optimisation of the total maximum current consumption $I_{OP,max}$ and the chip area A_{OP} . $I_{OP,max}$ is calculated with the help of (7), (8) and (14) to

$$I_{OP,max} \approx 4I_{D1,max} + (2d + e + 2g)I_{D1,max}^2 \quad (25)$$

Evaluation of the chip area gives

$$A_{OP} \approx 2K_C C_M + 8 \frac{W_1}{L_1} L_1^2 + 8 \frac{W_7}{L_7} L_7^2 + 8 \frac{W_{12}}{L_{12}} L_{12}^2$$

$$+ 8 \frac{W_{14}}{L_{14}} L_{14}^2 + 8 \frac{W_{17}}{L_{17}} L_{17}^2 + 4 \frac{W_{22}}{L_{22}} L_{22}^2, \quad (26)$$

where $1/K_C$ is the capacity per area. Figure 2 shows the chip area A_{OP} vs. the maximum current consumption $I_{OP,max}$ with d increasing from $d = 1000 \text{ A}^{-1}$ to $d = 9000 \text{ A}^{-1}$ where z is 0.4, 0.7 or 1.0, and choosing $L_1 = L_7 = L_{12} = L_{14} = L_{17} = L_{22} = 1 \text{ }\mu\text{m}$, $C_L = 20 \text{ pF}$, and $e_{nOP,min} = 2 \text{ nV}/\sqrt{\text{Hz}}$. The optimisation is hence done for the low-noise point with $I_{D1,max}$ of the programmable range. It is useful to have a relatively small g for achieving a small total current I_{OP} . Hence, g was set to a value of $g = 800 \text{ A}^{-1}$. For a small chip area, W_{17}/L_{17} should be small as well. Hence, $W_{17}/L_{17} = 5$ was chosen, which keeps M_{17} on. Each curve point represents a design point of the OpAmp with a defined maximum current consumption and a defined chip area.

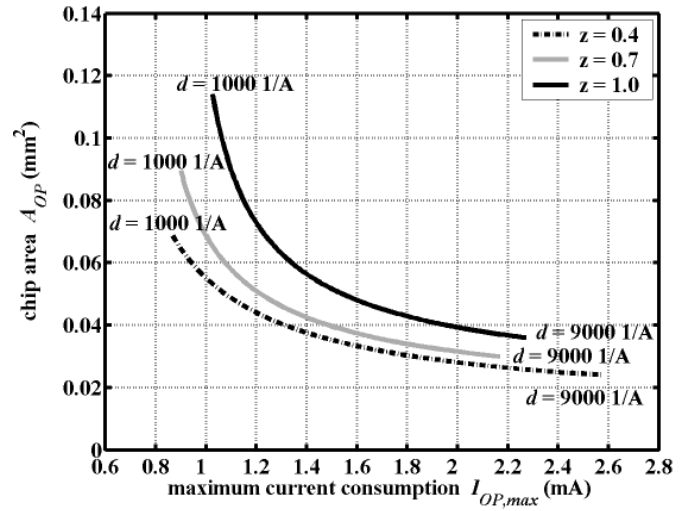


Figure 2: Trade-Off between chip area A_{OP} and the maximum current consumption $I_{OP,max}$.

Figure 2 offers a relatively simple possibility for the optimisation regarding chip area and current consumption. If an area-optimisation of the OpAmp is wanted, constant d together with the current consumption is chosen as large as possible. For a current-optimisation, constant d is made as small as possible together with a large chip area. For both cases a small z is of advantage.

For a joint optimisation, the product of A_{OP} and $I_{OP,max}$ from eqs. (25) and (26) is formed. The partial derivative of $A_{OP} \cdot I_{OP,max}$ is then performed to determine the optimal values for d and z , where $d_{opt} = 2924 \text{ A}^{-1}$ and $z_{opt} = 0.43$. The Miller capacitance and the W/L ratios of the respective transistors are determined with the help of these optimised values from eqs. (18), (20) and (22)-(24).

Equations (7), (8) and (14) define a quadratic relationship of I_{D12} , I_{D22} and I_{D17} to I_{D1} . Decreasing the current I_{D1} of transistor M_1 to decrease the power consumption of the OpAmp leads to much smaller currents I_{D12} , I_{D22} and I_{D17} . Hence, if I_{D1} is decreased, the transistors M_{12} , M_{22} and M_{17} go from saturation in subthreshold. To achieve a higher bias current for these transistors for a small I_{D1} , a linear fraction is introduced, which leads to

$$I_{D12} = aI_{D1} + dI_{D1}^2, \quad (27)$$

$$I_{D22} = bI_{D1} + eI_{D1}^2, \quad (28)$$

$$\text{and } I_{D17} = cI_{D1} + gI_{D1}^2, \quad (29)$$

where a , b and c are arbitrary factors. These factors are chosen such that the related transistors M_{12} , M_{22} and M_{17} are on for the low-power point. Figure 3 shows the linear-quadratic relationship for M_{12} .

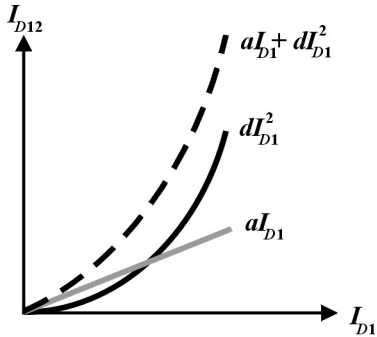


Figure 3: Linear-quadratic relationship of M_{12} .

III. RESULTS

The presented programmable Operational Amplifier was simulated in a 0.35 μm CMOS technology. The supply voltage for this technology is 3.3 V. The calculated W/L ratios of the transistors and the calculated Miller capacitance were the starting point for the dimensioning of the OpAmp, which was subsequently improved with the help of simulations. The factors a , b and c were determined by simulations to $a \approx 1$, $b \approx 9$ and $c \approx 0.08$.

Figure 4 shows the noise spectrum of the OpAmp for the low-noise point of the programmable range. The current consumption is then $I_{OP,max} = 3.9$ mA producing a minimal thermal noise of $e_{nOP,min} = 3.2$ nV/ $\sqrt{\text{Hz}}$ at a frequency of $f = 200$ kHz. The input noise is slightly higher than specified with $e_{nOP,min} = 2$ nV/ $\sqrt{\text{Hz}}$. The higher value is coming from neglecting the bulk voltages of the respective transistors in the theoretical model given in Section II. Nevertheless, the simulated input

noise shows a good agreement in first order with the specified value.

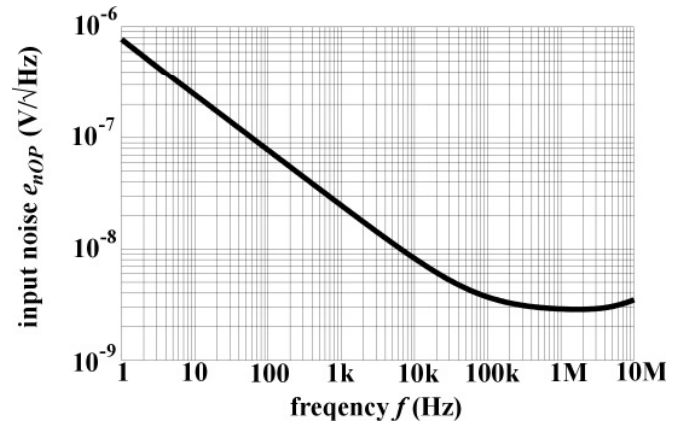


Figure 4: Noise spectrum of the OpAmp.

In Figure 5 the simulation results considering the power dissipation and the related input thermal noise at a frequency of $f = 200$ kHz is shown. The control current I_{ctrl} is changed from 1.5 μA to 150 μA producing a power consumption P_{OP} from 84 μW to 12.7 mW. Hence, the thermal input noise drops down from 31.2 nV/ $\sqrt{\text{Hz}}$ to 3.2 nV/ $\sqrt{\text{Hz}}$.

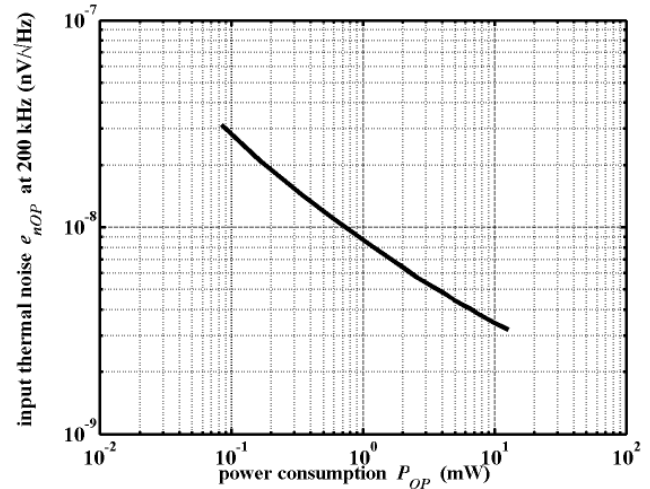


Figure 5: Thermal noise e_{nOP} vs. power consumption P_{OP} .

Figure 6 shows the unity gain phase margin φ_{res} vs. the power consumption P_{OP} for a load capacitance of $C_L = 20$ pF. Increasing the power consumption to decrease noise, the phase margin varies from 72° to 70° . The minimum phase margin is $\varphi_{res} = 69^\circ$ at a power consumption of $P_{OP} \approx 2$ mW. Hence, the phase margin variation is only $\Delta\varphi_{res} = 3^\circ$ over the whole range of programmability.

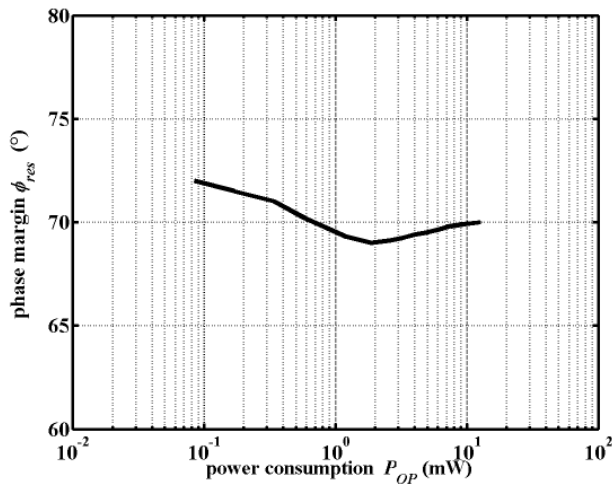


Figure 6: Unity gain phase margin ϕ_{res} vs. power consumption P_{OP} .

IV. CONCLUSIONS

An optimisation of a programmable Operational Amplifier was described. The optimisation is based on a systematic design procedure for realising programmability concerning noise and power consumption. A theoretical model was given achieving a constant phase margin for the whole operation range. The key problem of keeping the phase margin over the whole range of programmability is solved by using 2 additional current mirrors and a special biasing scheme of the OpAmp stages with a linear-quadratic relationship. Furthermore, the OpAmp is optimised regarding chip-area and current consumption. Simulation results for a 0.35 μm CMOS OpAmp show a variable power consumption from 84 μW to 12.7 mW, which reduces the input thermal noise from 31.2 $\text{nV}/\sqrt{\text{Hz}}$ down to 3.2 $\text{nV}/\sqrt{\text{Hz}}$. The phase margin

only varies between 69° and 72° and is therefore nearly constant for the whole range of programmability.

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