

# Design of a Reconfigurable, Differentially Driven Symmetric Inductor

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*Abstract*— A reconfigurable, differentially driven symmetric inductor is presented. This inductor is used in a differential  $LC$ -VCO, which is implemented in a  $0.35\ \mu\text{m}$  SiGe-BiCMOS-process. The output frequency of the  $LC$ -VCO covers twice the frequencies of the DECT- and the ISM-band (3.76 GHz...3.86 GHz respectively 4.8 GHz...4.967 GHz). The maximum simulated  $Q$ -factor of the inductor at differential excitation is about 10 at 3.86 GHz for the low frequency range and about 5.8 at 4.967 GHz for the high frequency range. The simulated phase noise of the differential VCO is  $-137\ \text{dBc/Hz}$  at 6.4 MHz offset for the low frequency band and  $-119\ \text{dBc/Hz}$  at 2.5 MHz offset for the high frequency band. For both frequency ranges the VCO consumes a supply current of 3.3 mA at a 3.3 V power supply voltage.

*Keywords*— Integrated spiral inductor; band-switching; voltage controlled oscillator.

## I. INTRODUCTION

Integrated inductors are important components in today's RF ICs for wireless applications like cordless phones or Bluetooth transceivers. This work presents a symmetric inductor, whose inductance  $L$  can be modified during operation by shorting the inner turn. The layout of the integrated, symmetric inductor is shown in Fig. 1. Ports 1 and 2 are the main connections of the differentially driven inductor, port 3 represents the common node and ports 4 and 5 are the contacts for shorting the inner turn.

This reconfigurable inductor is used in a differential  $LC$ -VCO, which operates at twice the frequency of the DECT- or the ISM-band (3.76 GHz...3.86 GHz respectively 4.8 GHz...4.967 GHz). The advantage of the doubled output frequency is a smaller chip area occupied by the inductor and an easier way of generating  $I$ - and  $Q$ -components for further modulation of the data signal. The paper shows that the designed differential  $LC$ -VCO with the integrated, symmetric inductor meets the phase noise requirements of the

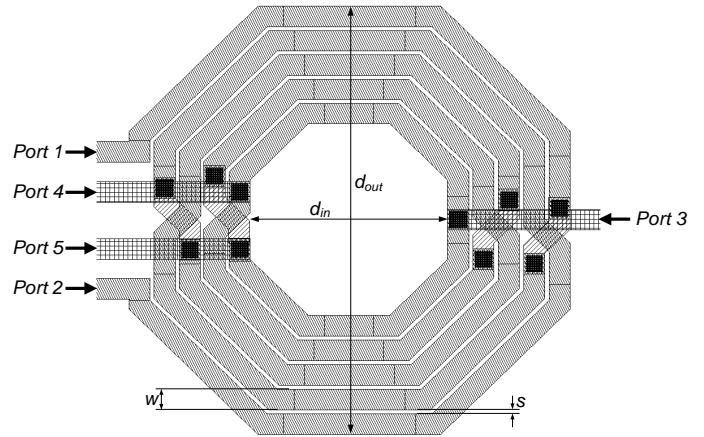


Fig. 1. Layout of the implemented inductor

DECT- and the ISM-band. Therefore, a reconfigurable inductor is a possible option for the design of a two-band  $LC$ -VCO.

## II. THE DESIGN OF THE INDUCTOR

During the layout of an integrated inductor for a desired application several design parameters have to be considered: the metal layers of the process used for the inductor, the shape of the inductor, the inner diameter  $d_{in}$ , the spacing  $s$  between the windings, the width  $w$  of the metal conductor and the chip area  $A$  occupied by the inductor (of course, the chip area depends on the number of turns  $n$ ). When using a reconfigurable inductor, the ratio  $n_2/n_1$  of the windings is one more parameter, which has to be chosen properly by the designer.

The quality factor  $Q$ , which can be approximated by  $Q \approx \frac{\omega L}{R}$ , is perhaps the most important parameter for an inductor and should be as high as possible. For an optimized, integrated spiral inductor the following set of rules should be applied during the design:

- Metal layers used for the inductor: This task depends on the metal layers, which are available in the

process. Generally speaking, the layers with the lowest sheet resistance should be used. If the layers are all of the same material, the layers with the lowest sheet resistance are the thickest ones. If the quality-factor of the integrated inductor does not meet the expectations, the parallel connection of several layers is a simple means of improving the  $Q$ -factor. In the technology used, the thickest layer is the top layer of the process. Therefore this layer is selected for the inductor windings. For the connections and for the crossings the lower layers are used (cf. Fig. 1).

- Shape of the inductor: The integrated spiral inductor should be laid out as circular as possible. Circular inductor geometries have a larger perimeter at the same radius than other geometries. Hence, with increasing number of sides  $N$  ( $N \rightarrow \infty$  represents the circular inductor) the resistance  $R$  as well as the inductance  $L$  of the spiral inductor increases. However, the  $Q$ -factor rises, because the inductance increases faster than the resistance. Considering the characteristics of the process used, several simulations were done with the ASITIC-simulator [1] to verify this rule. The used technology is restricted to multiple angles of  $45^\circ$ , thus an octagonal shape of the inductor is chosen.
- Chip-area  $A$ : Determining the chip area and thus the number of turns  $n$  of the spiral inductor is a trade-off process: The inductance  $L$  of a spiral inductor depends on the number of turns  $n$ . A first order approximation is given by:

$$L \sim n^2. \quad (1)$$

On the one hand an easy way to increase the inductance  $L$  is to increase the number of turns  $n$ . On the other hand the integrated inductor (and therefore the chip area) should be as small as possible to reduce the costs of the final chip production. Furthermore, with an increased chip area  $A$  the parasitic capacitance between the substrate and the metal conductors increases. This reduces the resonant frequency  $f_{res}$  of the spiral inductor. The presented inductor has an outer diameter of  $d_{out} = 210 \mu\text{m}$  and consumes a chip area of about  $A = 0.037 \text{ mm}^2$ .

- Inner diameter  $d_{in}$ : The inner diameter should be about 25 % to 45 % of the outer diameter  $d_{out}$ . It is obvious that the result of the design process is a hollow coil. If the inductor would be filled up with windings up to the center, these windings would contribute the smallest part to the complete inductance. Caused by the induced eddy currents of the outer windings, the resistance of the inner windings would be very high. This would degrade the  $Q$ -factor of the entire

inductor. Hence, the inner winding has a diameter of  $d_{in} = 94 \mu\text{m}$ .

- Spacing  $s$  between the windings: To achieve maximum magnetic coupling between the windings and thus a maximum inductance  $L$  of the coil, the spacing  $s$  between the windings should be as small as possible. The increased coupling capacitance is negligible in most cases. In the used technology the minimum allowed spacing  $s$  of the used thick metal is  $2 \mu\text{m}$ . This distance is chosen for the presented inductor layout.
- Width  $w$  of the metal conductor: Determining the optimum width  $w$  of the conductor is a trade-off process, too: On the one hand the width  $w$  should be as wide as possible to reduce the resistance  $R$  and thus to maximize the quality-factor  $Q$  of the inductor. On the other hand the width  $w$  should be as small as possible to reduce the skin effect in the conductor paths. Both effects have to be taken into account. The chosen width of the realized inductor is  $w = 10 \mu\text{m}$ .
- Ratio  $n_2/n_1$  of the windings: The ratio of the windings could be calculated from the ratio of the center frequencies  $f_{1c}$  and  $f_{2c}$  of the two frequency bands. The ratio  $n_2/n_1$  of the realized inductor is determined in the following:

$$\frac{f_{1c}}{f_{2c}} = \frac{4.8835 \text{ GHz}}{3.81 \text{ GHz}} = 1.282. \quad (2)$$

Using equation 1 and 2, the ratio  $n_2/n_1$  of the windings is defined by:

$$\frac{n_2}{n_1} = \sqrt{\frac{L_2}{L_1}} = \frac{f_{1c}}{f_{2c}} = 1.282. \quad (3)$$

Thus, the best integer winding-ratio for the reconfigurable inductor is chosen to be:  $n_2/n_1 = 5/4 = 1.25$ .

Table I summarizes the chosen parameters of the reconfigurable, symmetric inductor. The  $S$ -parameters of the implemented inductor have been simulated

TABLE I  
PARAMETERS OF THE RECONFIGURABLE INDUCTOR

Main metal layer	Thick metal
Shape	Octagonal
$A$	$0.037 \text{ mm}^2$
$d_{out}$	$210 \mu\text{m}$
$d_{in}$	$94 \mu\text{m}$
$s$	$2 \mu\text{m}$
$w$	$10 \mu\text{m}$
$n_2/n_1$	$5/4$

using the 2.5-D simulator *Momentum* of the design-environment *ADS 2003A* from Agilent Technologies. The inductance  $L$  and the quality-factor  $Q$  for both frequency ranges have been extracted for differential excitation out of the simulated  $S$ -parameters. The results are shown in Fig. 2. The  $Q$ -factor for the low frequency band is twice as high as the  $Q$  for the high frequency band. This is a result of the shorted inner turn. When simulating the symmetric inductor without the inner turn a quality factor of at least  $Q = 14$  could be achieved for the high frequency band.

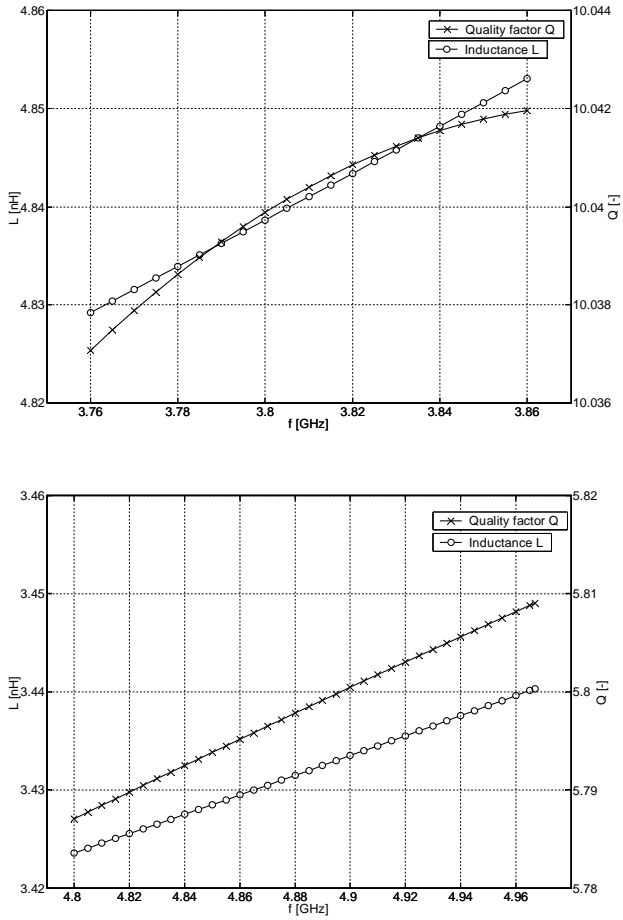


Fig. 2. Inductance  $L$  and quality-factor  $Q$  of the implemented inductor for the low and for the high frequency-band.

### III. THE IMPLEMENTED $LC$ -VCO

For the realization of the  $LC$ -VCO a differential topology with a cross-coupled pair of PMOS-transistors is chosen. The schematic of the VCO is depicted in Fig. 3. The current mirror is realized by the transistors  $m1$  and  $m2$ . The  $RC$ -low-pass fil-

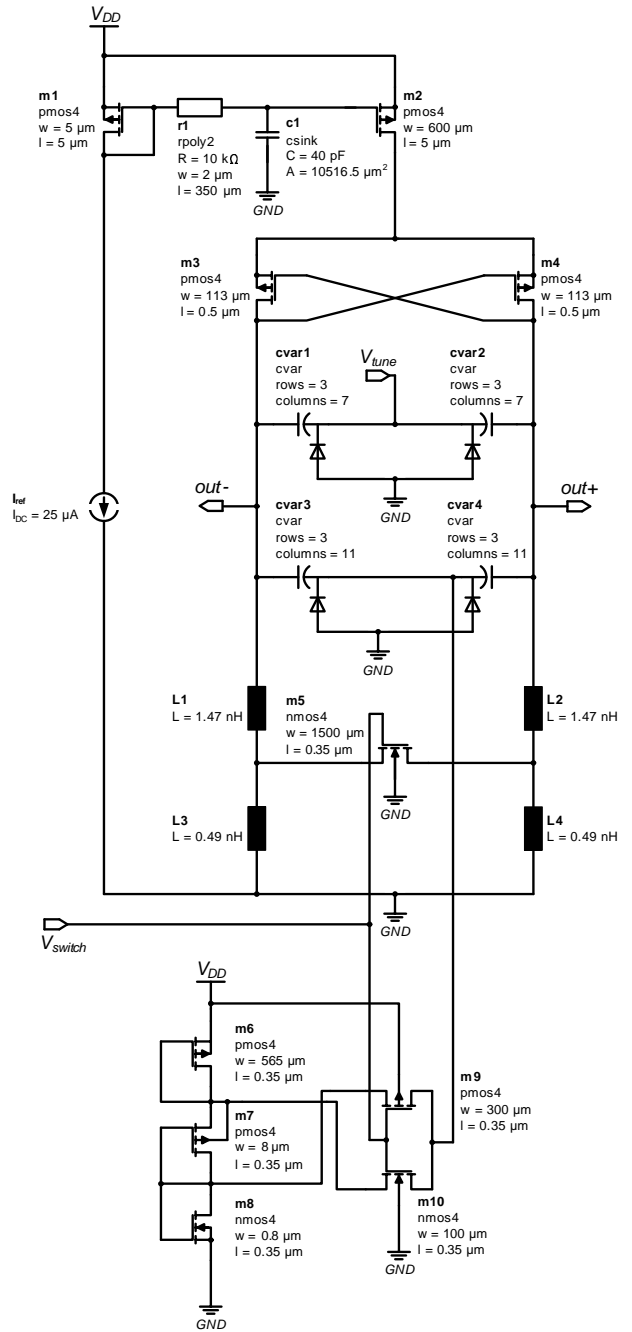


Fig. 3. Schematic of the differential  $LC$ -VCO

ter in between them decreases the noise injected into the entire circuit by the transistor  $m1$ .  $m5$  is the transistor shorting the inner turn of the inductor and is controlled by the voltage  $V_{switch}$ . The transistor has a  $W/L$ -ratio of about 4300 to minimize the additional resistance within the inductor and thus to maximize the quality-factor  $Q$ . The transistors  $m6$ ,  $m7$  and  $m8$  realize a voltage divider with the output voltages  $V_{low} = 1.47$  V and  $V_{high} = 2.6$  V.  $m9$  and  $m10$  represent a toggle switch, which is also con-

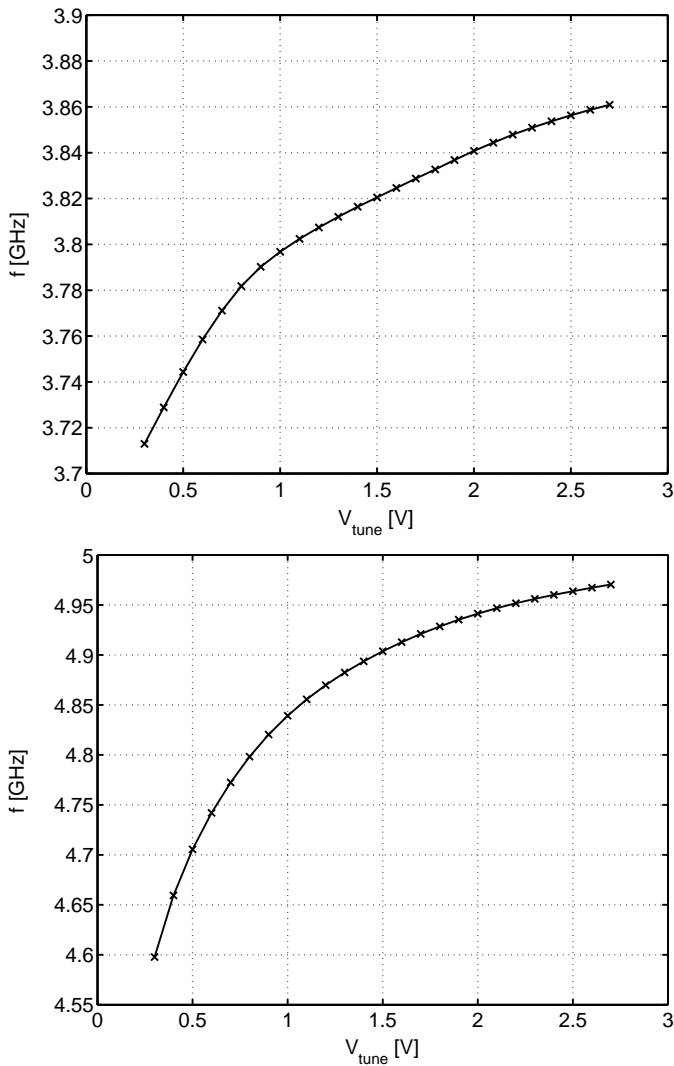


Fig. 4. Tuning-characteristic of the reconfigurable VCO

trolled by  $V_{switch}$ . The output of  $m9$  and  $m10$  controls the tuning-voltage of the varactors  $cvar3$  and  $cvar4$ , which are used for a more accurate adjustment of both frequency ranges.

Fig. 4 shows the simulated tuning-characteristic of the differential VCO. The required frequency ranges are achieved with a voltage tuning range of 2.04 V and 1.78 V for the low respectively for the high frequency band.

The results of the phase-noise simulations for the low and for the high frequency band are shown in Fig. 5. The thick, solid line represents the spectral mask of the DECT- respectively ISM-band adapted for the doubled output frequency. As it can be seen, the tuning voltage  $V_{tune}$  has a slight influence on the phase noise. At the most critical offset frequency  $\Delta f$  ( $\Delta f = 6.4$  MHz for the low frequency band and

$\Delta f = 2.5$  MHz for the high frequency band) the phase noise is 15 dBc/Hz better than the requirements for the low frequency band, but only 4 dBc/Hz better for the high frequency band. This mainly results from the quite different quality-factors  $Q$  of the reconfigurable inductor for the two frequency bands.

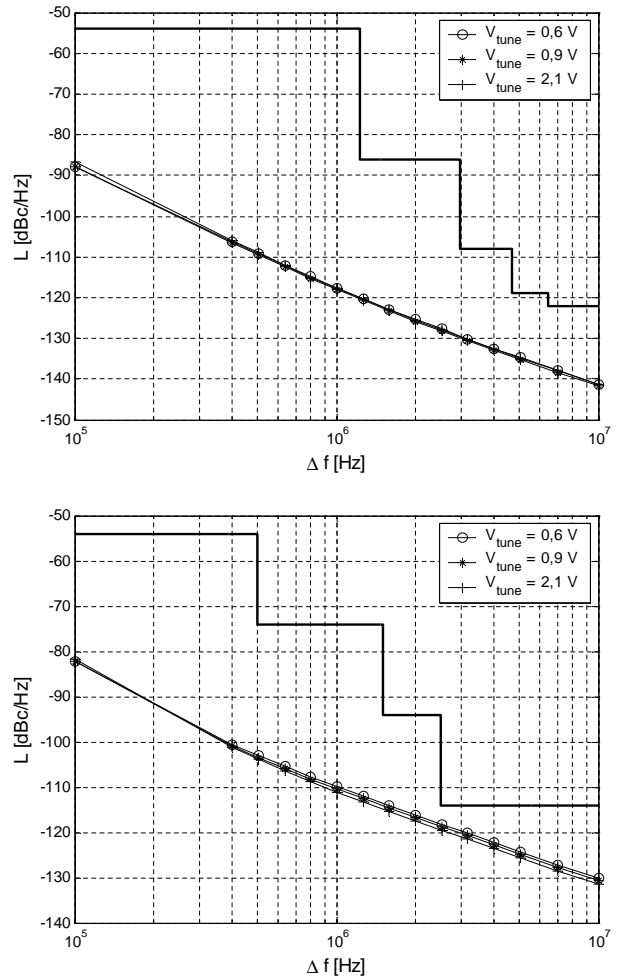


Fig. 5. Phase-noise simulations of the reconfigurable VCO

A widely-used figure of merit (FOM) for VCO performance ([2], [3]) is defined as:

$$FOM = \mathcal{L}\{\Delta f\} - 20 \log \left( \frac{f_0}{\Delta f} \right) + 10 \log \left( \frac{P_{dc}}{1 \text{ mW}} \right), \quad (4)$$

where  $\mathcal{L}\{\Delta f\}$  is the simulated phase noise at the offset frequency  $\Delta f$  from the carrier at  $f_0$ , and  $P_{dc}$  is the VCO power dissipation in mW. Table II summarizes the data for the calculation of the FOM for the low and for the high frequency band. For the calculation a tuning voltage of  $V_{tune} = 1.5$  V is chosen.

In [2] the FOMs for six previously designed VCOs

TABLE II  
FOM-DATA FOR BOTH FREQUENCY BANDS

	Low freq. band	High freq. band
$f_0$	3.821 GHz	4.904 GHz
$\Delta f$	6.4 MHz	2.5 MHz
$\mathcal{L}\{\Delta f\}$	-137 dBc/Hz	-119 dBc/Hz
$P_{dc} @ 3, 3 \text{ V}$	10.75 mW	10.74 mW
FOM	-182.2 dBc/Hz	-174.5 dBc/Hz

with non-reconfigurable inductors are denoted in the range of  $-189.4$  dBc/Hz and  $-176.6$  dBc/Hz. The simulated FOM of the presented, reconfigurable VCO is in about the same range.

A layout of the VCO was generated, extracted and backannotated. It is shown in Fig. 6. The dimensions of the layout are  $285 \mu\text{m} \times 337 \mu\text{m} = 0.096 \text{ mm}^2$ , in which the inductor takes about 40% of the chip area.

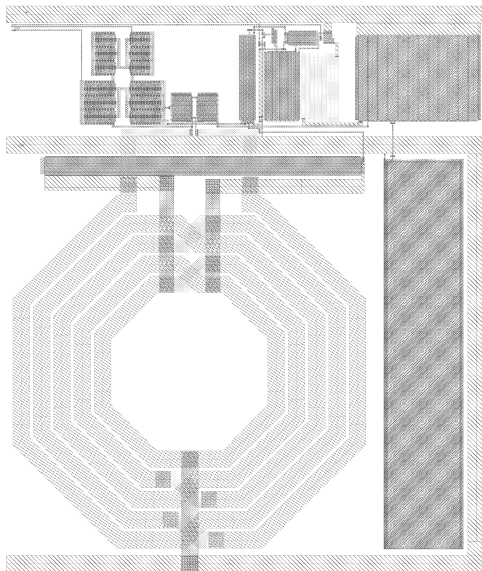


Fig. 6. Layout of the differential  $LC$ -VCO, dimensions:  $285 \mu\text{m} \times 337 \mu\text{m} = 0.096 \text{ mm}^2$ .

#### IV. CONCLUSION

A differential, dual band  $LC$ -VCO using a reconfigurable, symmetric inductor has been presented. The quality factor  $Q$  of the reconfigurable inductor has been about 10 at 3.86 GHz for the low frequency band and about 5.8 at 4.967 GHz for the high frequency band. The designed VCO has met the phase noise specifications of the DECT- and the ISM-band. The simulated phase noise at the most critical offset frequencies has been  $-137$  dBc/Hz at 6.4 MHz offset for

the low frequency band and  $-119$  dBc/Hz at 2.5 MHz offset for the high frequency band. The total area of the generated final layout has consumed a chip area of  $285 \mu\text{m} \times 337 \mu\text{m} = 0.096 \text{ mm}^2$ .

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