Surface Roughness of Contact Windows for Shallow Junction Formation

V. Gonda, A. Burtsev, T.L.M. Scholtes and L.K. Nanver

Delft University of Technology, DIMES-ECTM
Feldmannweg 17, POB 5053, 2600 GB Delft, The Netherlands,
Tel: +31 15 27 88837, Fax: +31 15 27 87369,
e-mail: v.gonda@dimes.tudelft.nl

Abstract— **In this study the surface roughness of the contact windows in which the laser annealed shallow junctions are formed is investigated. The contact windows are etched through a stack of an aluminium reflective masking layer on a silicon dioxide surface isolation layer. Comparisons are made between different types of Al and oxide layers, as well as different layer thicknesses. Various combinations of dry and wet etching are examined and the preliminary results show that the etch procedure can be tuned so that the resulting surface roughness is minimal.**

I. Introduction

Formation of shallow junctions is required for the future CMOS generations, where scaling down to dimensions below 0.13 microns will require source/drain junction depths shallower than 60 nm. Such junction depths can be achieved by implanting low energy dopants and activating them by excimer laser annealing, whereby a thin surface region is heated for such a short time that dopant diffusion is avoided. For high enough laser energy the Si surface will be melted and during the recrystallization process a very high level of dopant activation can be achieved. Since the melt temperature of amorphous Si is much lower than that of crystalline Si, the implanted, amorphized region determines the necessary laser energy. Also, the uniformity of the implanted region is important for the melt/recrystallization process. This uniformity will largely be determined by the roughness of the Si surface.

The surface roughness of the contact windows is investigated in this study. The contact windows are etched through an aluminium reflective layer on a silicon dioxide surface isolation layer to the silicon surface. Various material combinations and thicknesses are studied for the reflective and the isolation layer, respectively. The effect of dry etching as compared to wet etching is examined.

First an overview is given of the steps of the fabrication flow of the shallow junction diodes. Focusing on the etching step the ecthing experiment is described in the next section. Then we describe the surface roughness measurement methodology by means of AFM and the surface roughness parameters. Lastly the measurement results are described and a comparison is given.

II. Fabrication of diodes

The process flow for the fabrication of p^+n diodes is shown in Fig.1. The same procedure is used for the n^+p diodes with an p-substrate. The starting material is (100) silicon wafers with a surface doping of 10^{17} cm^{-3}. A 300 mm thermal oxide layer is grown followed by the deposition of 600 nm Al/Si(1%) as ELA reflecting masking layer. The diode and substrate contact windows are defined by plasma etching through the Al and oxide to the silicon. Before implanting the contacts, a 3 min 0.55 % HF dip-etch step is performed. In this step the native oxide in the contact windows is removed along with about 200 nm Al/Si. To avoid the formation of a new native oxide, the p-type and n-type regions are implanted immediately after the dip etch with BF_2^+ and As^+, respectively, with an energy of 5 keV and a dose of 10^{15} cm^{-2}, the ELA is performed with energies from 900 to 1100 mJ/cm^2. A 4 min HF dip-etch step is then performed to again remove the native oxide before the metallization. In this

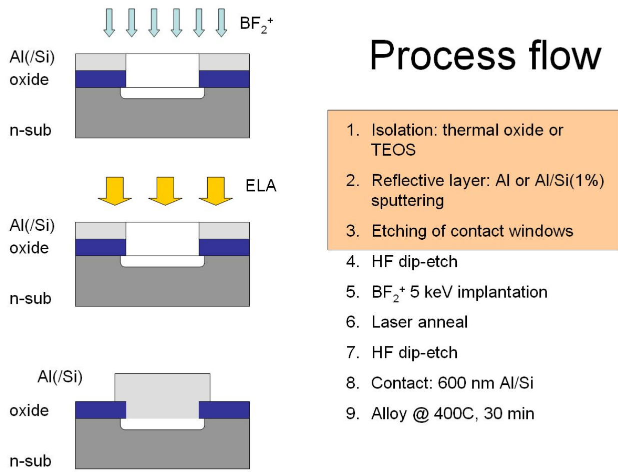

Fig. 1. Schematic of the process flow for fabrication of p$^+$n ELA diodes. The scope of the present study is highlighted.

step most of the Al/Si mask is removed, and the windows are contacted by sputtering and patterning of a new layer of 600 nm Al/Si(1%). A 400°C 30 min alloying step in forming gas completes the processing.

III. Etching Experiment

The influence of some of the process parameters such as the effect of alloying, the influence of dip-etching before implantation and the influence of the masking layer were evaluated previously by measuring basic diode characteristics [1]. Some of the diode characteristics suggest that the surface roughness of the contact windows has significant effect on the diode characteristics. Also, the uniformity of the implanted region is important for the melt/recrystallization process. This uniformity will largely be determined by the roughness of the Si surface.

There were two sets of experiments designed to determine the roughness after etching in the contact windows. Firstly the oxide quality, thickness and the reflective layer's thickness were varied, see the parameters in Table I. Results are shown for the four cases emphasized in the table in Section V.

Secondly the evolution of the roughness is studied during the etching processes, i.e. the surface roughness after Al removal in the oxide, deep in the oxide and finally at the Si surface. During the preparation of the experiment it was also possible to

TABLE I
Processes and parameters for experiment 1.

Reflective layer thickness (nm)	60	*100*
Reflective layer material	*Al/Si(1%)*	
Insulator layer thickness (nm)	30	*300*
Insulator layer material	*Thermal* oxide	*TEOS*
Etching	*dry*	*wet*
Al	RIE, chlorine	phosphoric
oxide	RIE, fluorine	BHF

TABLE II
Processes and parameters for experiment 2.

Reflective layer thickness (nm)	30	70	
Reflective layer material	pure Al	Al/Si(1%)	
Insulator layer thickness (nm)	300		
Insulator layer thickness	Thermal oxide		
Etching	hard landing	soft landing	wet landing
Al	RIE, chlorine		
oxide	RIE, fluorine, high power		
landing on Si	high power plasma	low power plasma	BHF

deposit pure aluminium in the lab. The thicknesses were chosen to meet the parameters of a process run conducted in parallel with the tests. Comparison of the surface roughness for plasma etching with and without soft landing, and also for wet landing is given. Summarizing the studied cases:

Case Surface roughness of

1) Oxide, after Al layer etched off by plasma
2) Oxide, before landing, high power plasma
3) Si, high power plasma
4) Si, low power plasma (soft landing)
5) Si, wet etched (wet landing)

IV. Surface Roughness Parameters

The surface roughness is measured by atomic force microscopy (AFM) in the laboratory. The scanned base area was 5 x 5 m^2 for all the measurements. The pre-processing of the data consists of compensating for waviness or any background envelope or skewness. Then the surface parameters were determined over the whole field, excluding

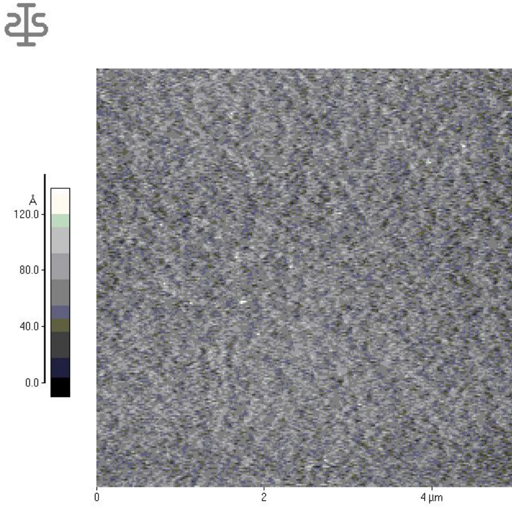

Fig. 2. The oxide surface after the reflective layer etched off.

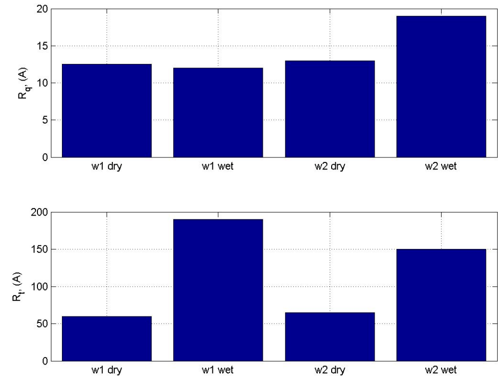

Fig. 3. Dry etch (w/ soft landing) to wet etching. w1 is Al/Si + thermal oxide, w2 is Al/Si + TEOS layers on Si.

extreme peaks in case. The following roughness parameters are determined: average roughness, root mean square roughness and total roughness.

The average roughness is the area between the roughness profile and its mean surface, or the integral of the absolute value of the roughness profile height over the evaluation area. The average roughness is defined over an area by

$$R_a = \frac{1}{A}\int_A |z - z| dA, \quad (1)$$

where A is the surface area, z is the height parameter, the overscore denotes the mean value.

The root mean square is a common statistical parameter describing the scatter, and it is formulated for the surface roughness measurements by

$$R_q = \sqrt{\frac{1}{A}\int_A (z - z)^2 dA}. \quad (2)$$

The total roughness describes the whole range of data over the measured surface,

$$R_t = |\max z - \min z|. \quad (3)$$

Equations 1 - 2 are used to define the scatter as a roughness parameter, and often used together with Eq. 3, which would also reveal seldom high peaks or low valleys.

V. Results

The first experiment results are shown in Fig. 3. The RMS roughness, R_q values are very close to each other in any parameter combination of the first set of experiments. Here results are only shown for the highlighted parameters in Table 1. Note that all values are very small, which means that both wet etching and dry etching with soft landing result in a very smooth surface. However comparing the total roughness values reveals that higher peaks (lower valleys) are found on the surfaces in case of wet etching. Indeed, the etching did not go smoothly due to the wet etching of the Al/Si reflective layer, probably some Si precipitates from the Al/Si separated on the Si surface. Also wet etching has an unfavorable effect on the small feature sizes, due to its isotropic behavior.

The evolution of the surface roughness during plasma etching in the oxide layer is shown in Fig. 4. At this step the Al layer is already etched off. The total roughness, R_t is divided by 10 to match the scale of the other parameters. The remaining oxide thickness was 30 nm and 16 nm for wafer 3 and 4, respectively. In general it shows that the deeper the penetration the smoother the surface is, due to the fact that approaching the silicon interface, and the etching rate is smaller in a deeper hole.

The final surface quality for different etching is shown in Fig. 5. Hard landing is etching the oxide with a high power plasma down to the silicon surface. Soft landing is a two step process, where

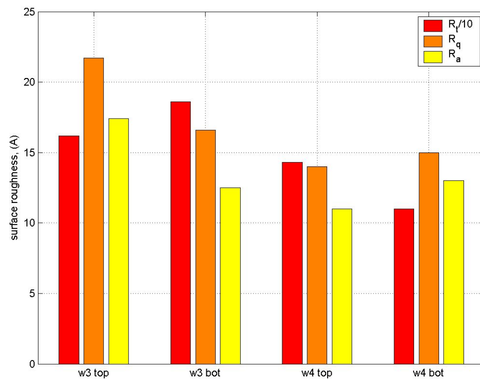

Fig. 4. Surface roughness in the top and bottom of the oxide layer with plasma etching. w3 is pure Al + thermal oxide, w4 is Al/Si(1%) + thermal oxide on Si.

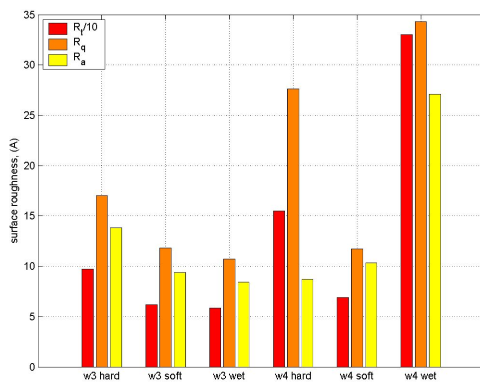

Fig. 5. Hard, soft and wet landing compared. w3 is pure Al + thermal oxide, w4 is Al/Si(1%) + thermal oxide on Si.

the plasma energy is lowered before reaching the Si substrate, and in general it results into a smoother surface. Wet landing is a two step process again, where the high power plasma etching is followed by a wet etching step in buffered hydrofluoric acid (BHF). A short wet etching step is also for the following implantation step. According to the results it can increase the surface roughness when Al/Si is used as a reflective layer.

VI. Conclusion

The surface quality is studied for contact openings created by etching through a stack of layers. The most favorable combination is a pure Al reflective layer, plasma etching with soft or wet landing.

References

[1] L. K. Nanver et al., *Electrical Characterisation of Silicon Diodes Formed by Laser Annealing of Implanted Dopants*, Proc. ECS 2003, Vol. 14, pp. 119-130.