

# FSK Demodulator Topologies for Ultra-low Power Wireless Transceivers

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*Abstract*— Personal communications require wireless nodes, which can transmit and receive reliably data under huge power constraints. Higher levels of integration and reduction of power consumption can be achieved using a zero-IF architecture together with a wideband BFSK modulation scheme. Unfortunately FSK techniques performances degrade sharply in the presence of frequency offset. In this paper a comparison between potentially low power BFSK demodulation architectures is presented based on high level models. In depth analysis of four potentially low power demodulators shows that the architecture, which can assure rejection of large static offset with minimum increment in hardware complexity is the ST-DFT based demodulator. Use of this demodulator will allow great reduction in power consumption avoiding acquisition and tracking of the offset at the receiver side.

## I. INTRODUCTION

The market for wireless connectivity has been growing rapidly in the past few years. A number of standards have been developed to satisfy the requirements of various parts of this market. These systems have unique characteristics and engineers will face new implementation challenges. The most severe design constraint is the limited amount of energy available for a wireless node. Beside this challenge, low cost and small size are two important features for a product that wants to reach the largest part of the consumer market.

Hardware minimization can be achieved by using a zero IF architecture, which eliminates the image-reject filter and other IF components, enabling a monolithic transceiver. One of the core blocks in a transceiver is the demodulator. In spite of its lower hardware complexity, the zero-IF architecture suffers from some special problems like DC offset and  $1/f$  flicker noise coming from CMOS transistors. Among the various ways to cope with such problems, the most straightforward way is to remove the low-frequency portion of the downconverted signal's spectrum by a highpass filter (HPF). However to avoid to cut a large portion of the signal energy, and to use simple a HPF filter it is important that the spectrum of the signal

is placed sufficiently far away from DC. For these reasons a non-coherent sideband binary frequency-shift-keying (BFSK) is a simple and robust form of digital modulation when the bandwidth requirements are not overly stringent like in transceivers for low data-rate applications.

From a power point of view, while analog circuits do not scale linearly down with technology scaling, digital circuits consume lower power at every new technology scaling. Therefore reduction of power consumption can be obtained by shifting complexity from the analog world to the digital world. FSK demodulators are simple to be implemented and they give a major advantage in terms of power consumption at the transmitter side due to the possibility to use non-linear amplification thanks to the intrinsic constant envelope of the modulation format.

Unfortunately, FSK shows limits when the frequency offset is nonzero, which is the normal case in practical applications due to imperfections in the local oscillator. Therefore if the demodulator cannot cope with this offset, the frequency instability should be corrected with an Automatic Frequency Control (AFC) system, before the signal can be correctly demodulated. This will increase the hardware complexity at the receiver side and therefore the overall power consumption.

The objective of this paper is to study the effect of frequency offset on different FSK demodulators under additive white Gaussian noise (AWGN) channel using simulations. To do so, four demodulators are thoroughly analyzed in the reminder of this paper and developed theory verified against simulations.

## II. BFSK DEMODULATION

Among all the demodulator architectures, four of them, suited for ultra-low power implementation, have been chosen and their performances have been simulated using Simulink models under different frequency offsets in a AWGN channel. These four types of demodulator are:

- Arctan-differentiated demodulator (ADM) [1]
- Correlation demodulator [2]
- Digital cross-differentiate multiply demodulator (DCDM) [3]
- Short-time DFT (ST-DFT) demodulator [4]

Another widely used digital demodulator is the zero-crossing demodulator. Unfortunately in [5] it has been shown that when the frequency offset is equal to the 6% of the data rate, the SNR degradation reaches 4.8 dB. In the field of low data-rate applications, this will limit the maximum uncorrected frequency offset, without significant degradation in the BER performances, to a few hundreds of Hertz, which is quite difficult to achieve in practice without an AFC system.

#### A. Arctan-Differentiated Demodulator

In this demodulator topology, the FM discriminator is followed by an Integrate-and-Dump (IaD) circuit and by a decision circuit, which retrieves the transmitted data. The block diagram of this demodulator

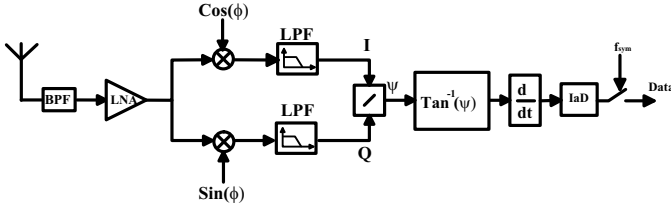


Fig. 1. Conventional Arctangent receiver

is shown in Fig.1. The received signal is first downconverted to a complex baseband signal to obtain the In-phase (I) and the Quadrature-phase (Q) signal components and then these components are used to retrieve the transmitted information. The I and Q components are:

$$\begin{cases} s_I(t) &= -\frac{A(t)}{2} [\cos(2\pi f_d \int_{-\infty}^t m(\tau) d\tau)] \\ s_Q(t) &= -\frac{A(t)}{2} [\sin(2\pi f_d \int_{-\infty}^t m(\tau) d\tau)] \end{cases} \quad (1)$$

where  $A(t)$  is the carrier frequency amplitude,  $f_d$  is the frequency deviation,  $m(\tau) = \sum_{n=-\infty}^{n=+\infty} a_n d(\tau - nT_s)$  is the transmitted signal with  $a_n = \pm 1$ , and  $d(t)$  the rectangular pulse over a symbol time  $T_s$ . Now, taking the ratio between the Q signal and the I signal and extracting the arctangent function it is possible to recover the signal information. The output of the inverse tangent block is the following:

$$\phi(t) = 2\pi f_d \int_{-\infty}^t m(\tau) d\tau \quad (2)$$

The transmitted signal is then retrieved by differentiation of  $\phi(t)$ , which can be performed in the digital domain subtracting one sample from the previous one, or by passing  $\phi(t)$  through a filter that approximates the response  $H(\omega) = j\omega$ . The IaD block and the decision block will retrieve the digital transmitted data. In the case in which the signal passes through an AWGN channel, remembering that the output of the discriminator is the derivative of the phase in (2) ( $\dot{\psi} = d\psi(t)/dt$ ), and considering that the IaD filter integrates over one symbol period, the output of the IaD is [6]

$$\Delta\psi = \Delta\phi + \Delta\eta + 2\pi N \quad (3)$$

where  $\Delta\phi$  is the signal component,  $\Delta\eta$  is the continuous phase component and  $2\pi N$  is the click noise component due to spikes at the discriminator output when the SNR is below the threshold point, in a symbol period. When a frequency offset is present then an additional phase term appears in (3):

$$\Delta\psi = \Delta\phi + \Delta\eta + 2\pi N + \Delta\theta \quad (4)$$

where  $\Delta\theta$  is the offset induced phase difference. If we consider a noiseless environment then it is easy to notice from (4) that, supposing a digital one has been transmitted, a negative frequency offset equal to  $f_d$  and the threshold of the decision block placed at zero,  $\Delta\psi = 0$  and the BER will approach 50%.

#### B. Correlation demodulator

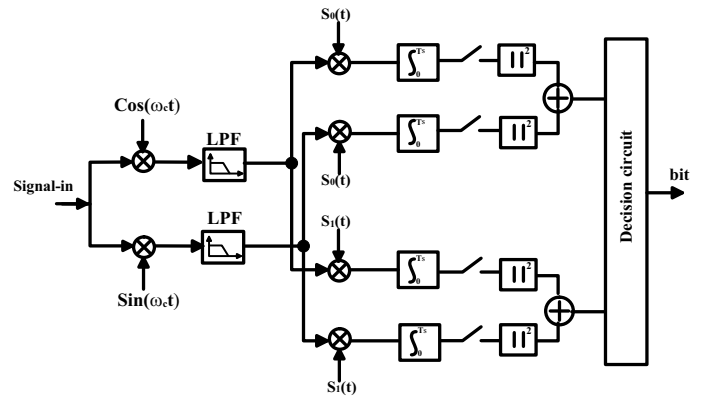


Fig. 2. Non-coherent correlator receiver

It is known that the optimum FSK detector is the correlation detector. In the real case, this correlation detector is not widely used due to its high complexity. In [2] a new correlation type detector has been proposed, which reduces the complexity of the system, avoiding to use the multipliers, which are replaced by

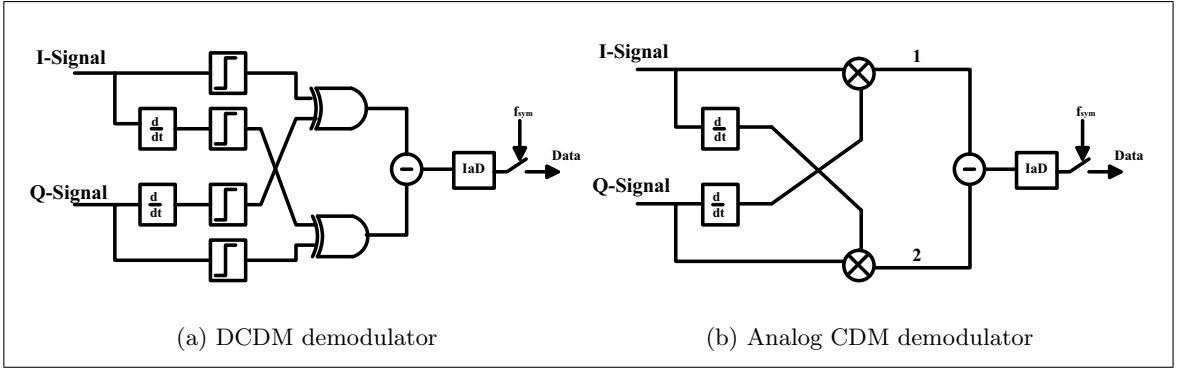


Fig. 3. Cross-differentiate-multiplier demodulator

simple XNOR logic ports. Nevertheless no data is provided when the incoming data and the local oscillator at the receiver side are not perfectly synchronized in frequency. A block diagram of a correlation demodulator is shown Fig.2.

It can be proved [7] that, in the presence of frequency offset, the detector matched to the incoming signal suffers from a signal attenuation equal to

$$\alpha = \frac{\sin^2 \pi \rho}{\pi^2 \rho^2} \quad (5)$$

where  $\rho = f_{\text{off}} T_s$ , with  $f_{\text{off}}$  the frequency offset and  $T_s$  the symbol period.

Furthermore, energy leakage exists from the correlator matched to the wanted signal to the other correlators. While this leakage can be ideally reduced to zero by displacing the FSK tones far apart, it is impossible to recover from the energy loss in the correlator matched to the wanted signal. Indeed, when  $\rho = 1$ , the term in (5) goes to zero. Therefore, no more energy is collected by the detector matched to the incoming signal and the BER is close to 50 %.

Therefore considering low data rate applications, the maximum residual offset should be less than 300 Hz, which requires, in practice, offset calibration at the receiver side.

### C. Digital cross-differentiate multiply demodulator

The cross-differentiate multiply demodulator has been largely used for FSK detectors in pager applications and a block diagram of a classical analog cross-differentiate and multiply detector is depicted in Fig.3(b). Realizing the derivative of a signal and two multipliers in the analog domain can be quite hard bringing to large power consumption and increased hardware complexity.

Therefore new topologies, still based on the cross-differentiate-multiply principle, have been developed

in order to reduce the hardware complexity and therefore the power consumption [3]. One of these topologies is depicted in Fig.3(a). Indeed if a zero IF architecture is used, the I and Q signals can be easily digitized and the derivative can be obtained by simple subtraction between two consecutive samples. Furthermore the complex analog multiplier can be replaced by a XOR logic port, which is used as one bit multiplier. Considering the simple analog representation given in Fig.3(b), and considering for the I and Q signal the expressions given in (1), then the signals at point 1 and 2 in Fig.3(b), with a constant signal amplitude, are

$$\begin{cases} s_1(t) = \frac{A^2}{4} \cos^2[2\pi(f_d \int_{-\infty}^t m(\tau) d\tau + f_{\text{off}} t)] \\ \quad \times 2\pi(m(t)f_d + f_{\text{off}}) \\ s_2(t) = -\frac{A^2}{4} \sin^2[2\pi(f_d \int_{-\infty}^t m(\tau) d\tau + f_{\text{off}} t)] \\ \quad \times 2\pi(m(t)f_d + f_{\text{off}}) \end{cases} \quad (6)$$

From (6) it is clear that when  $f_{\text{off}} = \pm f_d$  and  $m(t) = \mp 1$ , the BER should approach 50%. Even though (6) suggests the possibility of cancelling the frequency offset via proper encoding, it is easy to see that the presence of integrated noise (which has not been considered in (6)), will make the task not easy due to the fact that the output of the IaD stage is a stochastic variable.

### D. Short-time DFT demodulator

This demodulator is based on the Short-time DFT algorithm and has been proposed for low earth orbit (LEO) satellite communication systems [4].

A block diagram of a ST-DFT receiver is depicted in Fig.4. The Analog-to-Digital Converter (ADC) will work at low frequency due to the zero-IF architecture, thus minimizing the power consumption. All the processing to demodulate the incoming signal can be per-

formed in the digital domain, which has the potential to be very low power. The algorithm applies differen-

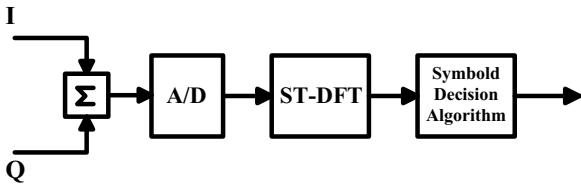


Fig. 4. ST-DFT demodulator

tial encoding. Therefore when the information bit "1" is transmitted, the modulation frequency is shifted respect to the previous symbol. If the information bit "0" is transmitted the modulation frequency remains unchanged.

At the receiver side, supposing perfect synchronization between transmitter and receiver, ST-DFT is applied on  $N$  samples of the incoming signal. Due to the noise, different peaks will be present in the spectrum including the tone of the transmitted signal. Let's call  $f_{dec}^{(m-1)}$  the decided frequency for the symbol  $m - 1$ . Let's suppose that  $t$  peaks are present in the ST-DFT of the symbol  $m$ . Then if the absolute value of the difference between the  $i$ -th peak and  $f_{dec}^{(m-1)}$  is less than  $2f_{res}$ , where  $f_{res}$  is the FFT resolution, then the decision algorithm will output a logic zero. If the difference  $\in [2f_d - 2f_{res}, 2f_d + 2f_{res}]$  then the decision circuit will output a logic one. If none of the previous conditions are met, then the peak is disregarded as a noise peak and the algorithm is applied to the following peak.

It can be seen that this simple algorithm can easily track the offset. Indeed, supposing that the decided frequency at the  $(m - 1) \times T_s$  time is  $f_{dec} = f_d + f_{off}$ , where  $f_{off}$  is the offset frequency and  $f_d$  is the frequency deviation, then when the information bit "1" is transmitted we have at the receiver side:

$$|\Delta f| = |-f_d + f_{off} - (f_d + f_{off})| = 2f_d \quad (7)$$

where  $\Delta f$  is the frequency difference between the  $m$  and the  $m - 1$  symbol. As can be seen from (8) the offset cancels out. When the information bit "0" is transmitted, the detected frequency difference is:

$$|\Delta f| = |f_d + f_{off} - (f_d + f_{off})| = 0 \quad (8)$$

Again the frequency offset cancels out.

### III. SIMULATIONS AND RESULTS

For all the demodulators a data rate of 1 kbps has been chosen together with a modulation index

$m_{index} = \frac{f_d}{D} = 8$ , where  $D$  is the data rate. Furthermore because of the sideband FSK modulation employed the effect of the HP filter is negligible and it will be neglected in the following analysis.

Both the AD and DCD demodulators use the phase information embedded in the signal to recover the transmitted data. Indeed the derivative of the phase of the incoming signal can be approximated by using the I and Q signals from the following equation:

$$\frac{d}{dt}(\phi(t)) \propto i(t)\frac{d}{dt}q(t) - q(t)\frac{d}{dt}i(t) \quad (9)$$

which is exactly the same operation performed in the DCDM demodulator (see Fig.3(b)).

It can be proven that these demodulators exhibit a threshold effect and therefore the input SNR should be high enough to allow the demodulator to work above the threshold requiring data pre-filtering.

In the case of the ST-DFT demodulator, the FFT length has been chosen equal to 1024, the filters at the transmitter side and at the receiver side have been chosen to be raised-cosine filter with roll-off factor equal to one. The window function is a Hanning window with a duration of two symbols.

From Fig.5(b) it can be seen that the correlation demodulator is quite weak when a frequency offset exists between the incoming signal and the local oscillator. Due to their similarities, the DCDM and the ADM demodulators exhibit same performances. As can be seen from Fig.5(a), when the offset exceeds 3 kHz, the BER exceeds 5%. For these demodulator topologies an AFC system is required.

Furthermore it can be noted that, when the frequency offset is equal to the frequency deviation, the BER is close to 25 % when a real noisy channel is considered. This can be easily understood by considering a system in which the SNR is high enough to guarantee a negligible BER. In this case, the probability that an error occurs, under a certain frequency offset given a transmitted symbol, can be approximated by a gaussian probability distribution (when a AWGN channel is considered). Now the probability that an error occurs can be expressed by the following equation:

$$P_{error} = P_{error|1}P_1 + P_{error|0}P_0 \quad (10)$$

where  $P_{error|1}$  is the probability of error given a transmitted symbol "1",  $P_{error|0}$  is the probability of error given a transmitted symbol "0",  $P_1$  is the probability that a "1" has been transmitted and  $P_0$  is the probability that a "0" has been transmitted. The probability that a symbol "one" or a symbol "zero"

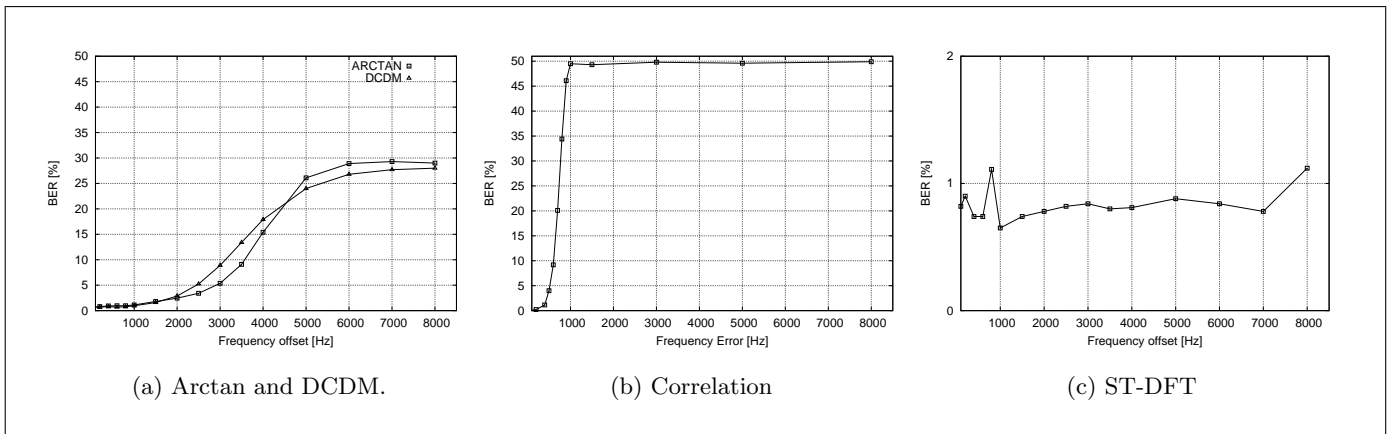


Fig. 5. BER vs frequency offset with  $E_b/N_0 = 12dB$

are transmitted is the same and equal to 0.5. The conditional probability in (10) can be easily derived by looking at Fig.6 in the particular case in which the frequency offset is equal to the frequency deviation. In this case we can approximate the probability of having an error given a transmitted symbol "one" to zero, while the probability to have an error when a symbol "zero" is transmitted is 0.5. Indeed looking at Fig.6 we can see that half of the gaussian curve is in the right half-plane. This means that due to the offset, when a symbol zero is transmitted, the receiver detects a positive voltage and assumes a "one" has been transmitted. On the other side, due to noise, it can happen that the output voltage sometimes is negative (grey portion) and a correct decision is made. Therefore, from (10) the probability of error, when white gaussian noise is added is around 25 % as shown in Fig.5(a).

On the other hand looking at the performance of the

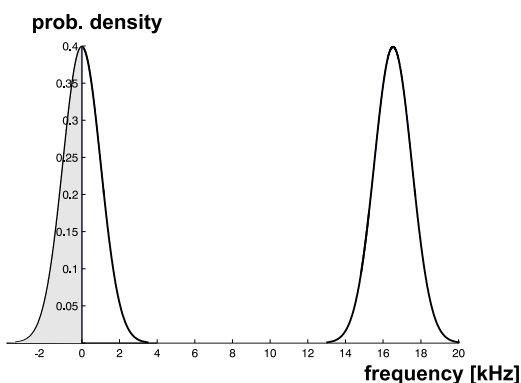


Fig. 6. conditional error probability distribution for "zero" and "one" symbol under frequency offset condition

ST-DFT demodulator it is possible to see its robustness against static frequency offset in a range that can be extended well above the 8 kHz shown in Fig.5(c).

Furthermore due to its simplicity and thanks to the zero-IF topology, which will require an ADC working at low frequency, it is possible to achieve huge reduction in the power consumption by performing all the demodulation in the digital domain using a low-power dedicated DSP.

#### IV. CONCLUSIONS

In the new era of personal communications, the energy available for a wireless node is the limiting factor. The path to reach a fully integrated, autonomous wireless node, passes through the minimization of hardware complexity and power consumption at all the levels. One of the key blocks in a transceiver is the demodulator. While FSK modulation together with a zero-IF architecture can simplify the RF part of the transceiver, it suffers from a huge degradation in BER when frequency offset is present. To avoid increase of hardware complexity and power consumption at the receiver side it is important to choose a demodulator which can cope with large frequency offsets. A study of several potentially low power FSK demodulator architectures has shown that the ST-DFT algorithm can easily reject static offset, avoiding the use of offset acquisition and tracking circuits at the receiver side. Furthermore the complexity in the analog front-end is shifted to the digital domain where it is possible to take the maximum benefit in terms of power consumption from technology scaling. This will greatly simplify the receiver architecture, which will result in a higher level of integration and in a reduction of the overall power consumption.

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