Die-to-Die Variations of a mm-Wave CMOS VCO

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***Abstract* — A mm-wave VCO tunable from 41 to 44.5 GHz (8% tuning range) is presented. It utilizes a differential tuning mechanism based on varactors and fixed MIM capacitors. Fabricated in a bulk CMOS 65nm technology, it consumes 3.6 mW and exhibits a phase noise of –106 dBc/Hz at 1 MHz offset from a 41.2 GHz carrier. The resulting FOM is –192.7 dBc/Hz, which is the best reported value for VCOs operating above 40 GHz. Twenty-nine samples are measured to analyze die-to-die variations of the VCO and results are presented.**

***Index Terms* — CMOS integrated circuits, Millimeter wave oscillators, Phase locked loops, Phase noise, Voltage controlled oscillators.**

I. INTRODUCTION

Millimeter wave Voltage-controlled oscillators (mm-VCOs) are key building blocks of advanced wireless systems. Broadband WPAN at 60 GHz ISM band, automotive radar sensors at 76 GHz and imaging applications at 94 GHz are some examples of such systems. Low power consumption, high output power, low phase noise and wide tuning range are important requirements for mm-VCOs.

MM-wave VCO design poses numerous challenges. At these frequencies, varactors, which are invariably used for tuning LC-VCOs, become the limiting factor for the overall tank quality factor. Furthermore, the value of the required passives is of the same order as parasitic capacitances and inductances. Therefore, accurate models of passives are vital for achieving correct oscillation frequency. In addition, layout dependent parasitics also become a critical problem.

Numerous integrated CMOS VCOs operating above 40 GHz have been reported [1]-[5]. In order to boost the oscillation frequency and improve quality factor of passives, high-resistivity substrates and SOI CMOS is being used [1]-[2]. However, these technologies require extra processing steps, thereby increasing the cost. Similarly, special layout techniques for transistors and passive devices, to minimize parasitics, have been demonstrated [4]. In this paper, a 44.5 GHz complementary cross-coupled LC VCO is presented. MIM capacitors are used to boost the quality factor of the capacitive part of the tank. Differential tuning is adopted to improve phase noise performance. Chip layout has been carried out carefully to avoid unnecessary parasitics. The VCO has been implemented in a 65nm bulk CMOS LP (low power) technology.

II. VCO CIRCUIT DESIGN

The VCO circuit is shown in Fig. 1 (a). A complementary cross-coupled architecture is chosen for this design. As compared to NMOS-only VCO, the complementary structure provides higher transconductance at a given current, which results in faster switching and larger output amplitude. In addition, it demonstrates superior rise- and fall-time symmetry, resulting in less upconversion of 1/f noise [6].

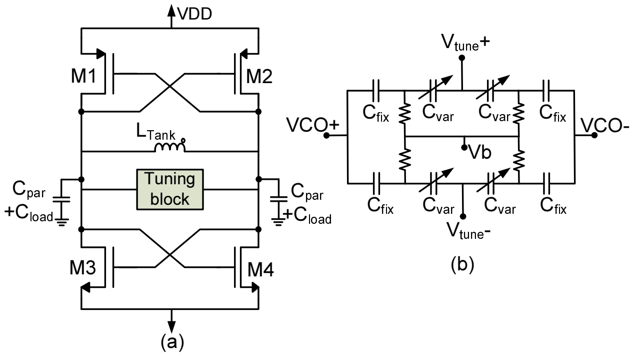


Fig. 1. (a) Complementary cross-coupled VCO, (b) Tuning circuit

The transistors M1 to M4 form the active part of the VCO. A ratio of two is chosen between negative transconductance and losses of the tank, to ensure reliable startup. In order to match the transconductance of PMOS and NMOS transistors, the former has twice the width. The resonator is composed of a single turn octagonal shaped inductor and a combination of varactors and fixed MIM capacitors. An output buffer is included for measurement purposes. The differential outputs use 50Ω transmission lines to the bond-pads.

III. RESONATOR AND OUTPUT BUFFER

At mm-wave frequencies the required inductors are small and exhibit a reasonably high quality factor (Q). In contrast, quality factor of the capacitive part, i.e. the varactors becomes the dominant factor. The quality factor of a LC tank (Q_{Tank}) is given by $1/Q_{Tank} = 1/Q_L + 1/Q_C$ where Q_L and Q_C are quality factors of the inductor and capacitors that make up the tank. In case, Q_L is much lower than Q_C, which is generally the case for frequencies up to a few gigahertz, improving Q_L leads to a higher Q_{Tank}. However, at mm-wave frequencies the quality factor of the capacitor (Q_C) is significantly lower than Q_L [3]. Thus, more design effort should be invested in improving Q_C at mm-wave frequencies rather than improving Q_L.

The on-chip integrated inductor is a single turn octagonal shaped coil. It utilizes the thick top metal, to reduce series resistance, thereby increasing the quality factor. The inductor metal width and inner radius are 6µm and 15µm, respectively. The simulated inductance value is 95 pH, with a quality factor of 20 at 40 GHz. The area occupied by the inductor is 60x60 µm.

The tuning of VCO is achieved by combination of accumulation MOS (AMOS) varactors and fixed MIM capacitors (see Fig. 1 (b)). Metal-insulated-metal (MIM) capacitors exhibit high Q-factors (above 20) at mm-wave frequencies due to low intrinsic losses. Thus, using them in series with varactors improves the quality factor, at the expense of reduced tuning range. The C_{max}/C_{min} ratio of this setup is 2.1 and Q_C varies between 8.5 and 14.3. The reduced capacitance ratio due to MIM capacitors is not an issue, as the desired frequency tuning range is successfully achieved. The advantage on the other hand is that Q_C improves by approx. 40% as compared to a stand-alone varactor implementation.

In addition, some flexibility is achieved by connecting the lower terminal of the biasing resistors (Vb in Fig. 1(b)) to an external supply instead of grounding them. This provides an extra control voltage to cater parasitics and process variation. If the VCO is tuned single-endedly, common-mode noise can modulate the varactors, and appear as jitter and phase noise at the VCO output. Therefore, differential tuning is adopted for the capacitive part of the LC-tank to alleviate this problem [2].

A common-source differential stage is used as an output buffer, to make on-wafer measurements possible. In order to avoid loading of the VCO, the buffer is biased independently. This also helps in measuring the power consumption of VCO and buffer separately. The load resistance (silicided poly-silicon based) is 50Ω, to match it with the transmission lines as well as the measurement equipment.

IV. LAYOUT AND TECHNOLOGY

In order to reduce parasitics, layout is done carefully and compactly. The RF signal paths are kept as short as possible and narrow connecting lines are avoided to minimize resistive losses. Ground meshing is used underneath the RF paths. Decoupling capacitors are included for the voltage supplies. The differential outputs use 50Ω transmission lines (TL's) to the bond-pads. These TL's are coplanar waveguide based with lateral ground-plane consisting of all metal layers. The width of the TL is 5µm and spacing from the ground plane is 4.22µm.

The VCO is fabricated in TSMC bulk CMOS 65nm LP (low-power) process having six metallization layers. The process offers MIM capacitors and poly-silicon resistors. The measured f_T of NMOS and PMOS transistors is 140 GHz and 80 GHz, respectively. Due to bond-pad limitation the total chip area is 700 x 400 µm. However, the VCO core only occupies 100 x 100 µm. The chip micrograph is shown in Fig. 2.

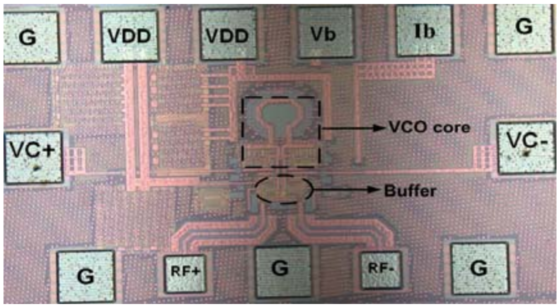


Fig. 2. Chip micrograph

V. MEASUREMENT RESULTS

The VCO was measured on-wafer using a RF differential probe (GSGSG) and a 180° hybrid coupler. An Agilent PSA series spectrum analyzer with phase noise functionality was used for spectral measurements. In order to suppress the noise coming from power supplies, dedicated filters are employed. In addition, common-grounds between the supplies and spectrum analyzer are eliminated. The lighting of the viewing optics is turned-off during measurement [2]. It is noticed that central alignment of the infinity probes (on the bond-pads) and

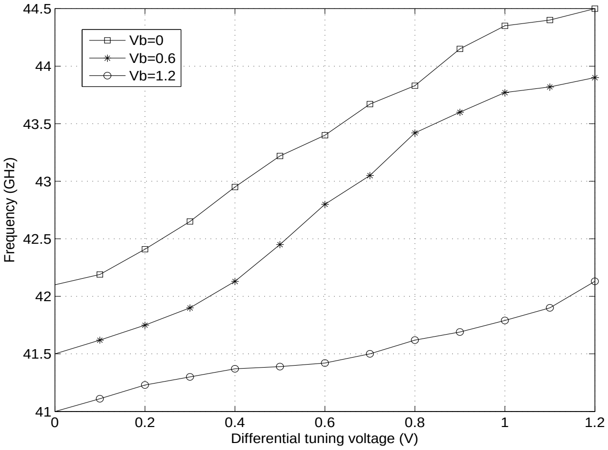


Fig. 3. VCO frequency tuning range

good probe contact yields stable and repeatable measurements.

The frequency tuning range (FTR) of the VCO is shown in Fig. 3, where output oscillation frequency is plotted versus differential tuning voltage for three bias voltages (Vb). The minimum and maximum measured frequencies are 41 GHz and 44.5 GHz (see Fig. 4), respectively, giving a tuning range of 8.1 %.

The VCO and output buffer consume 3mA and 5mA from a 1.2V supply, respectively. The total loss from the wiring cables, connectors and hybrid was measured between 6 and 8 dB over the entire frequency tuning range. After de-embedding this loss, the average differential output power delivered to a 50Ω load is between -2 and -6 dBm.

The measured phase noise of the VCO at 41.2 GHz is shown in Fig. 5. At 100 kHz and 1 MHz offsets, the measured values are -98 and -106 dBc/Hz, respectively. The commonly used FOM for VCOs is defined as $\mathrm{FOM} = L\{\Delta f\} - 20\log(f_o/\Delta f) + 10\log(P_{dc}/1\ \mathrm{mW})$, where $L\{\Delta f\}$ is the measured phase noise at frequency offset Δf from the carrier at f_o, and P_{dc} is the DC power consumption [1]. Using the above expression and measured phase noise at 1-MHz offset, a FOM of -192.7 dBc/Hz is achieved, which is the best reported FOM for VCOs operating above 40 GHz.

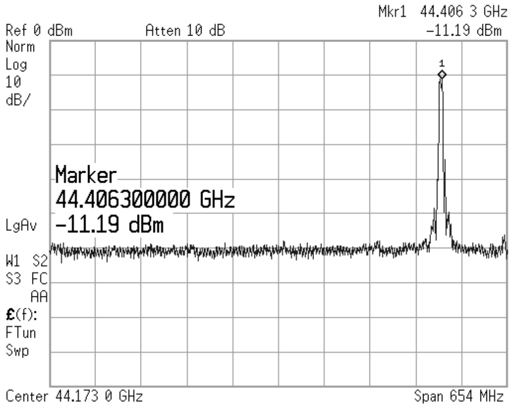
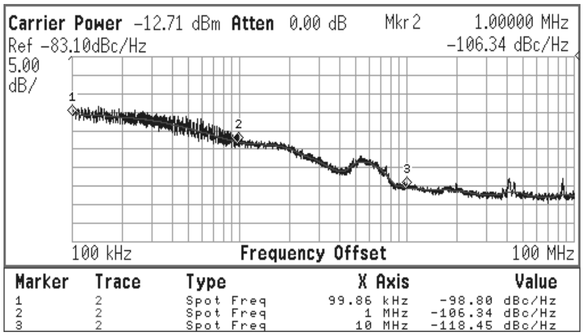


Fig. 4. VCO output spectrum at 44.4 GHz



Marker	Trace	Type	X Axis	Value
1	2	Spot Freq	99.86 kHz	-98.80 dBc/Hz
2	2	Spot Freq	1 MHz	-106.34 dBc/Hz
3	2	Spot Freq	10 MHz	-118.45 dBc/Hz

Fig. 5. VCO phase noise for a 41.2 GHz carrier

As VCO's, at a later stage, become a part of frequency synthesizers in wireless transceivers, their performance variation from die-to-die is undesirable. In order to analyze the spreading of the fabricated VCO, twenty-nine samples were measured. The measurement setup and DC conditions were kept constant in all measurements for a fair comparison. Fig. 6 shows the variation of VCO center frequency for three different bias voltages (Vb). Two corner samples did not work and were probably damaged during wafer fibbing. The measured standard deviation for the three bias voltages (0, 0.6, 1.2V) is 683 MHz, 590 MHz and 629 MHz, respectively.

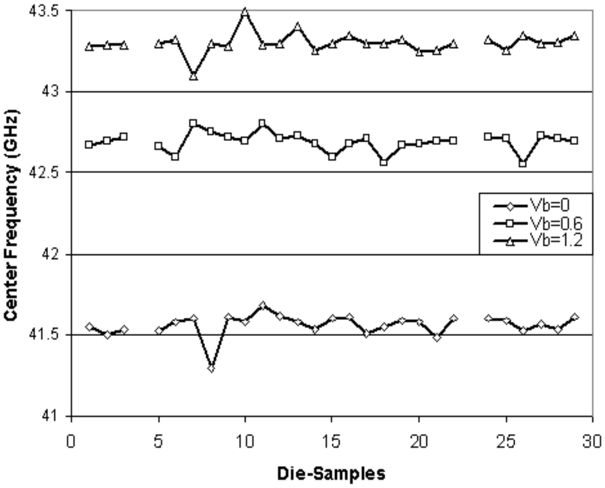


Fig. 6. VCO center frequency variation for different samples

The phase noise and output power variation is also measured. For each sample, the tuning voltage is set in such a way that the oscillation frequency is 41.2 GHz for all samples. Then the phase noise and output power are noted down and shown in Fig.7. The phase noise results show considerable variation, the mean value being -103.75 dBc/Hz with a standard deviation of 1.5 dBc/Hz. The mean output power, after de-emmbedding loss of the cables etc, is -4.6 dBm and standard deviation is 0.8 dBm.

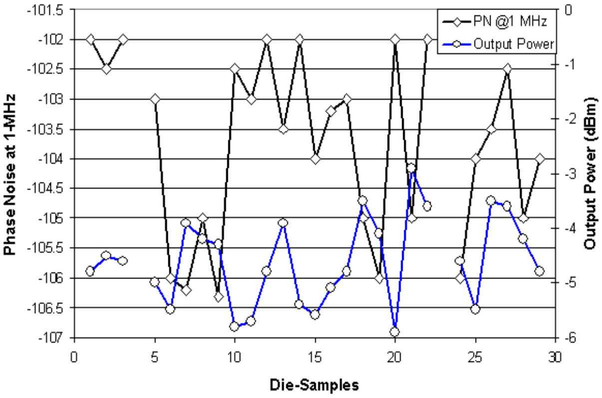


Fig. 7. Phase noise and output power variation

Table I compares, published state-of-the-art VCO's operating at mm-wave frequencies. The presented VCO has the lowest power-consumption (excluding output buffers) while achieving a reasonable frequency tuning range. The phase noise is better than reported SOI implementations in [1], [2].

V. CONCLUSION

A 44.5 GHz complementary LC cross-coupled VCO implemented in a 65nm bulk CMOS LP technology is presented. The use of MIM capacitors to improve Q_C, differential tuning to reduce phase noise and compact layout to minimize parasitics yields good measured results. The VCO has a FTR of 8% and dissipates only 3.6mW. The measured phase noise at 1MHz offset from a 41.2 GHz carrier is -106 dBc/Hz resulting in an excellent FOM of -192.7 dBc/Hz.

TABLE I

COMPARISON WITH PUBLISHED RESULTS

Ref. & Tech.	Freq. (GHz)	P_{dc} (mW)	FTR (%)	PN@ 1MHz (dBc/Hz)	FOM (dBc/Hz)
[1] 0.13µm SOI CMOS	40.7	11.3	15	-89	-170.6
[2] 0.12µm CMOS SOI	44	7.5	9.8	-101	-185
[3] 0.13µm CMOS	43	7	4.2	-90	-174.2
[4] 0.13µm CMOS	59	9.8	10.2	-89	-174.5
[5] 0.18µm CMOS	50	4	2	-96	-184
This work 65nm CMOS	44.5	3.6	8.1	-106	-192.7

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