Towards a Mixed-signal SoC Platform

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Abstract—**The designers cannot keep pace with the technology, which provides such massive amount of transistors. Time-to-market pressure and increased design complexity created what it is called a "design gap" [1]. As a solution to that problem the Platform-Based Design (PBD), based on the design-reuse methodology, has been proposed [2], [3].**

Moreover, it is true that in the System-on-Chip (SoC) design the analog part dominates the overall design time, cost and risk. The I/O interfacing by analog-to-digital and digital-to-analog converters (ADC's/DAC's) is a necessary part of every SoC system that has to communicate with the real (analog) world.

In this paper we propose the Mixed-signal FPGA (FPMA) platform as a solution to the described above problems. The FPMA platform is an extension of the purely digital FPGA platform with additional analog functions such as ADC's/DAC's, anti-alias filters, etc. Specifically, we present the feasibility of an ADC platform, based on the use of identical basic building blocks and we demonstrate several possible ADC architectures.

Keywords— **Platform-based Design; PBD; System-on-Chip; SoC; analog-to-digital; ADC;**

I. INTRODUCTION

A. Platform-based Design (PBD)

Every year the IC technology provides a higher transistor density, increasing approximately 60% per year. The designers cannot keep pace with it because the design efficiency (engineering skills, productivity of tools and methods) increases only around 20% per year [1].

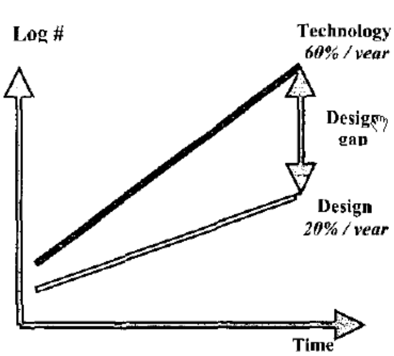


Figure 1: The design gap crisis [1]

Furthermore, time-to-market pressure and the masks' ownership cost drive us to more disciplined design styles. Figure 2 presents the natural evolution of design methodologies through time.

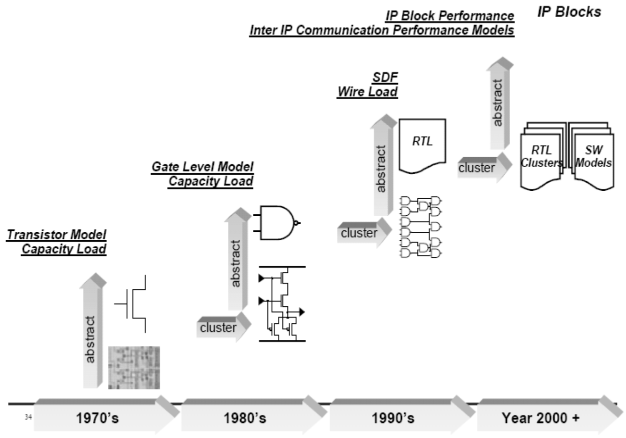


Figure 2: Evolution of the design methodologies [3]

As we can see according to cope with the increasing complexity, we adopt a design methodology, which lies in higher abstraction level and allows more massive design reuse, starting from single transistor reuse and reaching the level of IP block reuse.

However, as the complexity of the IC designs increases continuously and time-to-market becomes even more important, a new more advanced and higher in level of abstraction reuse methodology becomes imperative.

Therefore, as a natural progression of this line of thinking, the Platform-Based Design (PBD) has been proposed [2], [3]. It is a new design reuse methodology based on architecture reuse. A platform is a library of components that can be assembled to generate a design at that level of abstraction. These components can be divided in two categories: i) "Computational" blocks that carry out the appropriate computation function, ii) "Communication" components that interconnect the computational blocks. Each component of the library has a characterization in terms of performance parameters and functionality it can support. We call a *platform instance* a set of components that are selected from the library and their parameters are set.

Platforms allow design reuse from functional level down to circuit and layout level and, finally, real hardware level reuse.

Adopting a design reuse methodology, we have a series of advantages:

- We decrease the design risk since we use pre-defined and pre-characterized components.
- We reduce the system design effort and therefore the design cost and time
- We speed up time-to-market.
- We reduce test implications and test cost.

FPGAs (Field Programmable Gate Arrays) are a very successful example of platform that includes full hardware reuse. They are digital systems and the physical layer is decoupled from the functional layer. The system designer can make them functioning in conformity to the system specifications by programming the highly regular on-chip structures.

B. System-on-Chip (SoC)

The recent rapid progress of integrated circuit technology allows the integration of a whole system on a single ship. This trend finally implies the single-chip integration of analog and digital functions. Especially, with the rise of Personal Internet Products (PIP's), the quest for SoC integration becomes even more indispensable [4]. With the term Personal Internet Products, we referred to electronic systems, which are enabled by Internet, like cable modems, PDA's, cell phones, ADSL etc. (fig. 3).

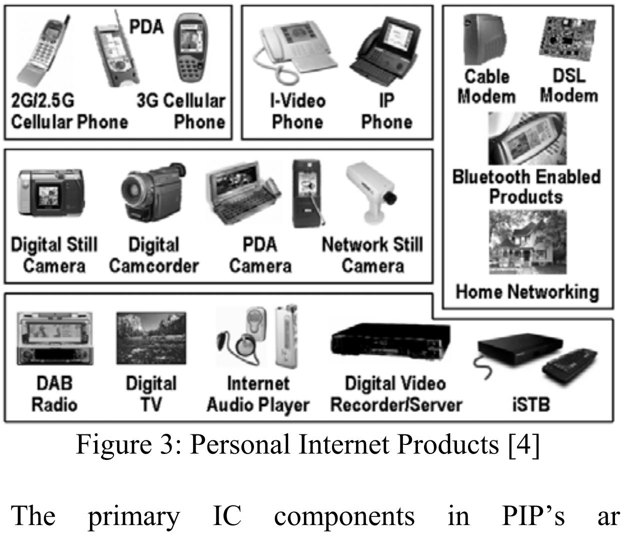


Figure 3: Personal Internet Products [4]

The primary IC components in PIP's are microprocessors and memory, but Digital Signal Processing (DSP) and analog functionality increase in importance. The reason behind this is that most of these products have real time analog input and/or output.

However, this SoC trend interferes with the design reuse and PBD methodology, as those analog/mixed-signal platforms are not available yet. This trammels the realization of truly SoC platforms and finally the design of the analog part dominates the design time, cost and risk.

The fundamental reason for that is that in the analog case the physical effects have so significant influence on the performance and functionality of the system, so that the physical layer cannot be decoupled from the functional layer. This rise a series of problems such as:

- The analog hardware are strongly coupled to the performance,
- It is needed a large set of analog functional blocks to cover the needs of specific system,
- There is strong influence between the analog blocks themselves and between the analog blocks and the interconnections.

Besides, the biggest challenge in implementing high performance analog systems in pure digital CMOS technologies is the low voltage environment. Furthermore, the absent of components, like capacitors, resistors, inductors, with good analog characteristics makes impossible the migration of existing analog designs to digital CMOS. Therefore, we should adopt a new approach that utilizes the benefits of the low voltage and low cost digital logic.

In this paper, we describe a way to apply the principles of the PBD in the design of an ADC platform. This platform aims to extend the functionality of the FPGAs. We present the basic Building Block (BB) that generates all the desired architectures and we describe its functionality. We propose the use of specific digital correction/calibration algorithms, according to ease the analog design. Finally, we demonstrate several ADC architectures that can be implemented using that BB.

II. ADC PLATFORM

A. The basic block

Figure 3 shows the symbol and the internal structure of the Basic Block (BB). The vector on the BB points the direction analog input/analog output and it consists of a flash sub-ADC, a sub-DAC, a subtraction block and a Sample & Hold Amplifier (S&H Amp).

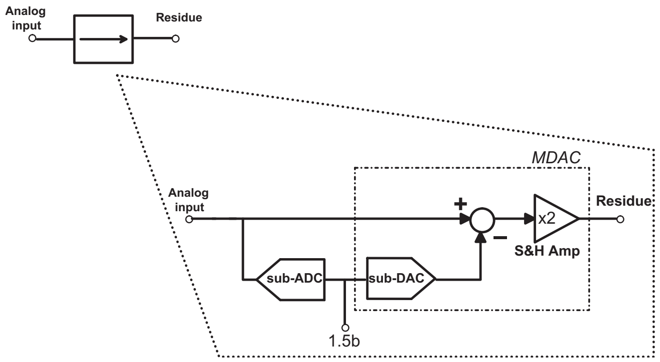


Figure 3: The basic block

Usually, the functions of digital-to-analog conversion, subtraction and S&H amplification are implemented in one single circuit called *multiplying DAC* (*MDAC*) and a closed-loop switched-capacitor realization of that circuit is employed. The resolution of every block is equal to 1.5b, which means effective resolution of 1b plus 0.5b reserved for digital correction [5].

Figure 4 shows the typical input-output characteristic of such a block:

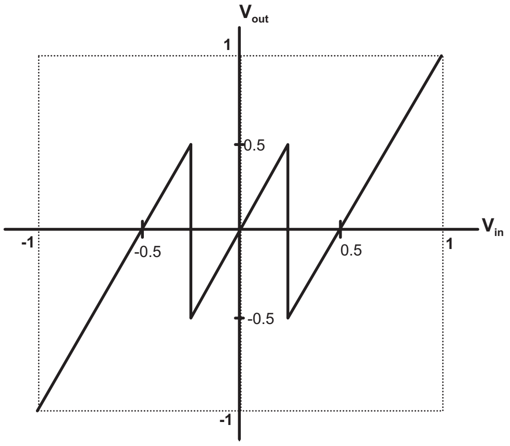


Figure 4: Basic block characteristic

The full-scale voltage is assumed equal to one.

Our choice to use identical BB's, according to generate the ADC platform, improves the modularity and flexibility, towards many combinations, while at the same time it ensures robustness. Furthermore, the utilization of a single block minimizes design risk and time and allows easier IP-reuse.

B. Digital correction/calibration algorithms

The utilization of this ADC platform into a high-performance FPGA permits extensive use of digital correction/calibration algorithms. We propose the use of three distinct techniques:

- *Digital correction* [5], which employing bit redundancy (0.5bit in our case), greatly relaxes the sub-ADC's comparators' offset specifications. Figure 5 shows the effect of comparators' offset to the block characteristic.

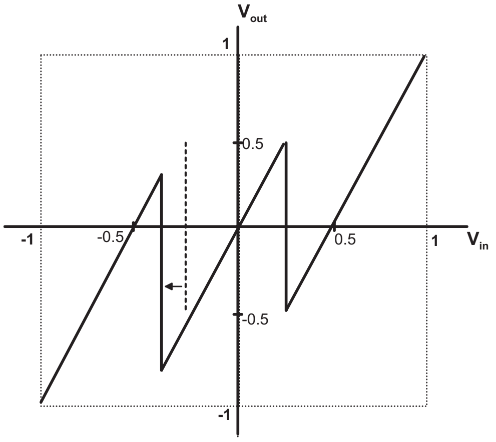


Figure 5: Comparator's offset

- *Digital calibration* [6], which employing stage redundancy, corrects offset and linear errors in sub-DAC and residue S&H amplifier. Figure 6 shows the effect of high amplifier's gain to the block characteristic.

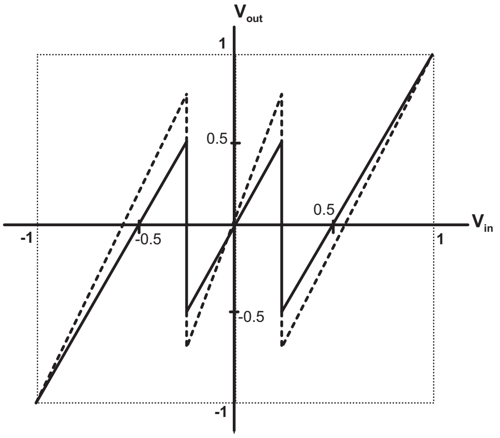


Figure 6: S&H Amplifier's high gain

- *Digital non-linearity calibration* [7], which using a digital algorithm, corrects static non-linearities of sub-DAC and residue S&H amplifier.

Using the above techniques, we essentially translate the analog precision problem into the digital domain. This is in line with the trend of the new technologies that offer higher speed, but worse voltage resolution. Furthermore, the digital systems become smaller and chipper, while the analog counterparts suffer from the low voltage environment. Therefore, several advantages arise due to translation of the analog problems to digital domain. We expect potentially power savings and/or speed improvements and it may help to overcome future scaling problems.

It is clear that the above correction methods relax the analog design and especially, the non-linearity calibration algorithm allows us to use open-loop residue amplifier, instead of the standard closed-loop realization. The potential of open-loop structures for high-speed applications has demonstrated [8], as well as the capability to achieve lower power dissipation for specific speed [7].

III. EXAMPLES OF SOME POSSIBLE ADC'S

A. Pipelined ADC

The pipelined architecture has been proven as the best choice for high accuracy and high-speed applications and, furthermore, it exhibits small area and low power dissipation.

Figure 7 shows how we can build a pipelined ADC as a chain of BB's. It is the typical pipelined architecture, constructed by identical stages.

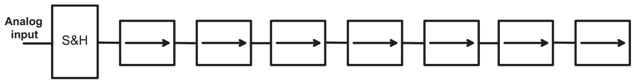


Figure 7: Pipelined ADC

The analog input is first sampled-and-held and then digitized by the sub-ADC of the first BB, resolving the most significant bits (MSBs) of the ADC. These bits are applied to the sub-DAC to produce an analog voltage, which is subtracted form the sampled-and held-input. The difference is amplified by 2 (scaled back to the full-scale) and it represents the residue. The analog output of the first BB is passed to the second BB as an input, while the first BB samples the next sample from the front-end S&H. The second and the rest of the BB's perform the same set of operations and at the end, the resolved bits are combined with digital correction [5] to yield the final output digital word of the ADC.

Taking into account the calibration/correction algorithm [6] we may use more stages that the desirable number of output bits. Using that algorithm, we have the possibility to under-design the BB's, with respect to the desired accuracy, and then to post-correct them, in the digital domain. For example, if we want 12b accuracy, we may design the blocks with 6b intrinsic accuracy and using 16 stages to reach the 12b accuracy [9].

B. Time-Interleaved Pipelined ADC

As described above the pipelined architecture is the most popular choice for high-speed/high-resolution application. Such specifications set strict requirements for the ADC and the design of it becomes very difficult. Therefore, the Time-Interleaved (TI) architecture has been proposed, which achieves high-speed operation by converting different analog samples in parallel using M identical ADC's (channels). The significant advantage due to this parallelism is the speed relaxation by M times on each channel. Thus, the design of each individual channel is much easier.

Figure 8 depicts the implementation of a TI ADC using identical BB's and a front-end S&H. For demonstration purpose, we employ a four channel TI ADC with six BB's per channel. Each channel is essentially a pipelined ADC.

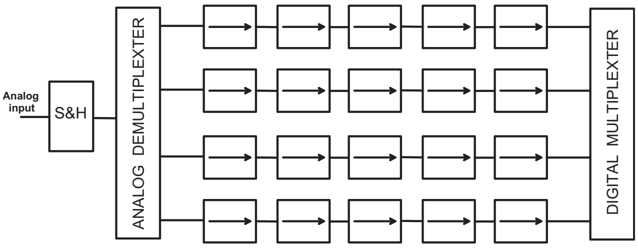
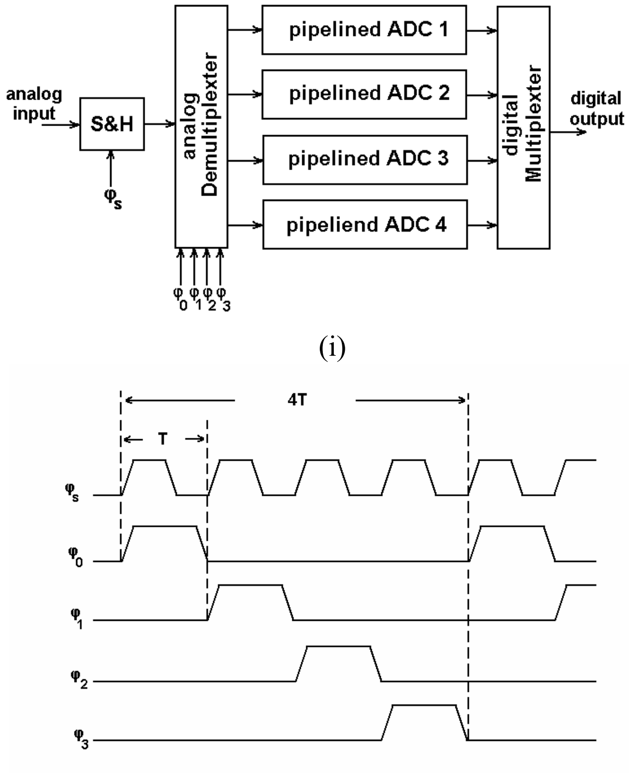


Figure 8: Time Interleaved ADC

Figure 9 shows the block diagram of that ADC, along with the clocking scheme. The front-end S&H operates at a sampling rate M=4 times faster that the rate of an individual chain that means, according to fig 9, φ_s clock is M=4 time faster than the φ_0-φ_3 clocks.



(i)

(ii)

Figure 9: (i) Block diagram of the TI ADC and (ii) clocking scheme

During operation, the analog demultiplexer selects each ADC chain in turn to process the input signal. The corresponding digital multiplexer selects the digital output of each ADC chain periodically and forms a high-speed ADC output.

Typical sources of errors are the *offset* and *gain mismatches* and *timing errors* between the channels of the TI ADC's.

- *Offset mismatch*: This mismatch causes a fixed pattern noise with peaks in the frequency domain with period of MT_s and the SNR degradation (noise power) is almost independent of the input signal.
- *Gain mismatch*: This mismatch causes, as the offset mismatch, fixed pattern noise with peaks in frequency domain every MT_s. The SNR degradation is independent of the frequency of the input signal, but it depends on the amplitude.
- *Timing errors*: We can identify two timing errors, namely, the *clock skew* (deterministic error), which degrades the SFDR and the *clock jitter* (random error), which degrades the SNR.

Several digital calibration/correction methods exist and partially correct the above-mentioned errors. Reference [10] uses digital background calibration techniques to overcome the effects of offset and gain mismatches between channels, while the reference [11] employs a digital algorithm to reduce the channel timing-errors effects, specifically the timing clock skew effects.

C. *Cyclic ADC*

Originally, the cyclic (or algorithmic) ADC has been proposed [12] having a single bit sub-ADC (essentially a comparator) and a single bit sub-DAC, fig. 10. We can easily recognize the similarities with the BB, fig. 3.

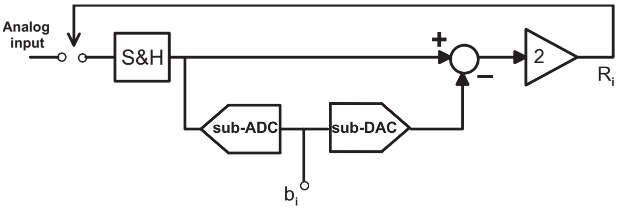


Figure 10: Cyclic ADC

The equation $R_{i+1} = 2R_i - b_i V_{ref}$ describes the implemented algorithm, where R_i is the residue, b_i the output bit of the sub-ADC (+1 or -1) and V_{ref} the reference voltage of the ADC.

Their key features are their potential for low-power and small area.

We can form a cyclic ADC, by using a front-end S&H and two BB's, fig. 11.

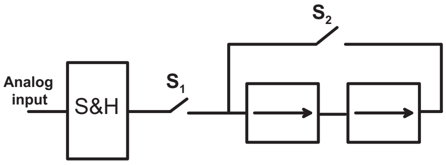


Figure 11: Cyclic ADC made of BB's

We can identify some differences compared to the original idea. We use two BB's instead of one, because when the analog output of a BB is valid the same BB cannot sample this output. Moreover, the BB has 1.5b resolution instead of 1b.

The operation of the proposed cyclic ADC has as follow: The switch S_1 switches on and the first BB samples the output of the front-end S&H. Consequently, this switch goes off and the S_2 turns on and remains on until the ADC resolves the complete digital word. As we have the complete word, the S_2 goes off and S_1 turns on to provide a new sample from the front-end S&H.

IV. CONCLUSIONS

In this work the feasibility of an ADC platform, suitable for implementation in an FPGA, has been demonstrated. The platform is based on the utilization of identical building blocks (BB's). We paid extra attention on the simplicity and the modularity of the BB, while at the same time we do not jeopardize the performance of the ADCs. We propose extensively use of digital calibration/correction algorithms, since the translation of the analog precision problem to the digital domain has identified as beneficial in terms of power, area and effectiveness.

We show the implementation of the BB and we present some ADC architectures that can be implemented using this BB. A wide area of performance specifications can be covered.

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