

Predictive analogue-to-digital converter for low-power electrocardiographic applications

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Abstract—A predictive A/D-converter for the acquisition and digitisation of electrocardiographic (ECG) signals is presented. The proposed converter is intended to be utilised in low-power ECG applications.

Index Terms—prediction, sigma delta converter, integrated circuits, bioelectric signals, digital prediction

I. INTRODUCTION

Low-power circuits become more important for mobile applications, especially for medical measurement devices. The amplitudes of biomedical signals are small, and therefore they have to be amplified into a comfortable and processable amplitude range. DC-offsets at the input of the amplifier limit the dynamic range because saturation might occur. In earlier concepts, DC-offsets at the input are disposed using a high-pass filter with a low corner frequency, which prevents saturation of the large gain input amplifiers. The drawback of an integration on chip is the fact that the capacities of the high-pass filter require a large fraction of the total chip area.

A proposed concept, which fulfils the requirements for low-power and low-cost circuits, and which is robust with regard to DC-offsets, is the concept of predictive signal processing [1]. The intention of predictive signal processing is to make use of previous knowledge of the input signal. The more the receiver knows about the signal, the less information has to be transmitted. Thus with predictive signal processing, signals can be handled on chip with reduced power consumption, data in storage and transmission can be reduced, and the amount of chip area can be decreased. Contrary to the approach exposed in [1], the proposed converter is completely integrable on-chip and consumes even less power.

II. PREDICTION

The conventional ECG-channel includes an analogue front-end [2], a high- and low-pass filter and a $\Sigma\Delta$ -A/D-converter, see Fig. 1. An improved concept [1] makes use of the linear Δ -modulation described in [3]. Fig. II shows this concept. Note a slightly different forward path and a predictive filter in the feedback loop, which completes the encoder to a closed loop system [1]. The predictor in Fig. II generates estimates of the input signal and delivers them to a subtracting input amplifier. The advantage is that the resulting predictive error signal can be amplified much more and the high-pass filter

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and the post-amplifier in Fig. 1 can be omitted. Restrictions for the inherent noise of the components in the system can be restrained, which leads to a lower power consumption.

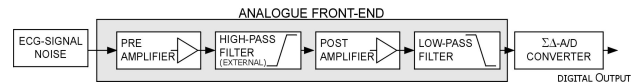


Fig. 1: Conventional channel for ECG-Signal amplification and A/D-conversion [1].

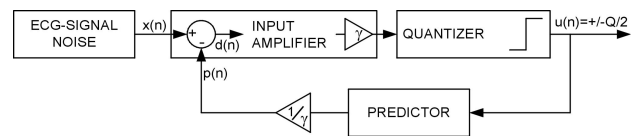


Fig. 2: Improved concept for the acquisition of ECG-Signals.

In order to calculate the prediction filter it is necessary to model the ECG-signal first. The signal can be modelled by using the power density spectrum and amplitude distribution of the ECG-Signal. The ECG-signal has an amplitude of approx. 1 mV and an average power of approx. $2 \cdot 10^{-8} \text{ V}^2$ [4].

For the sake of simplicity, a suitable model is a 1st-order Gauss-Markov-Process (AR_1) which is defined by

$$AR_1(z) = \frac{z}{z - h_1} \quad (1)$$

with

$$h_1 = e^{-\frac{2\pi f_c}{f_s}}, \quad (2)$$

where f_c is the corner frequency of the power density spectrum of an ECG-signal [1] (see Fig. 3) and f_s the sampling frequency. The corner frequency f_c is approx. 14 Hz. While

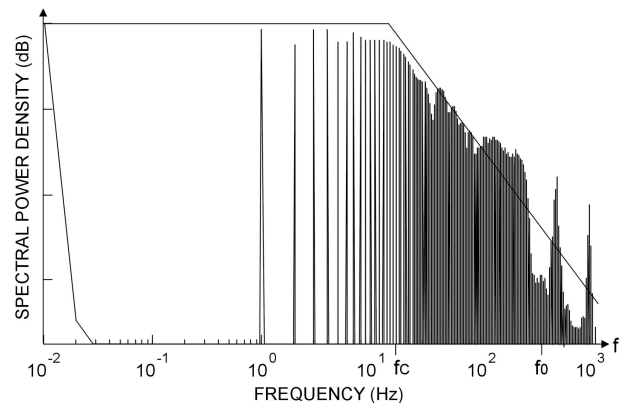


Fig. 3: Spectral power density of an ECG-Signal [4].

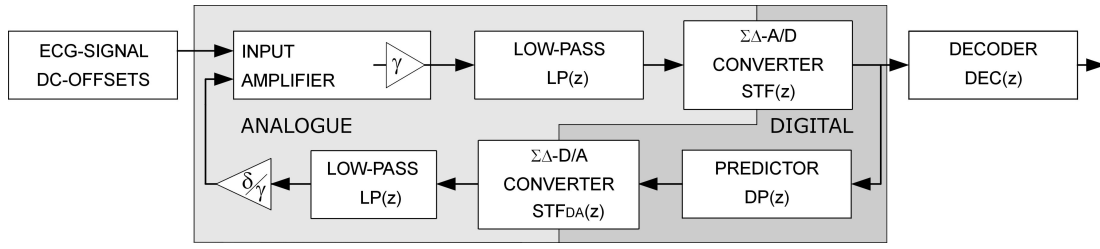


Fig. 4: Complete encoder for ECG-Signal amplification and A/D-conversion divided into digital and analog parts.

an $AR_2(z)$ process seems to fit the experimental spectrum a bit better, we adopt the AR_1 model because it is easier to handle when computing the prediction filter.

The optimum predictor $DP(z)$ is derived from the transfer function

$$\begin{aligned} E_{XD}(z) &= \frac{D(z)}{X(z)} = \frac{1}{1 + DP(z)} \\ &= AR_N^{-1}(z) = 1 - \sum_{j=1}^N h_j z^{-j}, \end{aligned} \quad (3)$$

where $X(z)$ is the input signal and $D(z) = X(z) - P(z)$ is the difference signal between the input signal and predicted signal $P(z)$, see Fig. II. The optimum predictor [1] then is determined as

$$DP(z) = \frac{h_1}{z - h_1}. \quad (4)$$

III. ARCHITECTURE

The system works as a closed loop encoder with an analogue front-end [2] and a $\Sigma\Delta$ -A/D-modulator in the forward path, and a digital prediction filter followed by a $\Sigma\Delta$ -D/A-converter in the feedback path (see Fig. 4). The analogue front-end consists of a large gain input-amplifier with a gain of γ and a 2^{nd} -order low-pass filter working as an anti-aliasing filter. An additional damping factor δ is introduced for ensuring the stability of the system. The encoder consists of discrete- and continuous-time components. Therefore, every single block has to be transformed into the z -domain in order to perform the dimensioning process.

IV. CIRCUIT DESIGN

In the following subsections A-F, the transfer functions of the system and its components are compiled.

A. Analogue Front-End

The low-noise and low-power amplifier [2] has a constant amplification of γ (see Fig. 4) and is followed by a low-pass filter $LP(z)$. The low-pass filter is realized in Sallen&Key-form with Bessel-characteristics, but in the calculations it is approximated by a 2^{nd} -order low-pass filter with the same corner frequency. The corner frequency f_{lp} of the low-pass filter $LP(z)$ can be determined, as a rule of thumb [1], by

$$f_{lp} \approx f_s/15. \quad (5)$$

The low-pass filter is calculated as

$$LP(z) = \left(\frac{1 - z_{lp}}{z - z_{lp}} \right)^2 \quad (6)$$

with

$$z_{lp} = e^{-\frac{2\pi f_{lp}}{f_s}}. \quad (7)$$

B. Digital Prediction Filter

As mentioned in Sec. II, the optimum predictor $DP(z)$ is derived from the inverse transfer function $E_{XD}(z)$. From Fig. 4, $E_{XD}(z)$ is determined as

$$E_{XD}(z) = \frac{D(z)}{X(z)} = \frac{1}{1 + \delta DP(z) LP(z)^2 STF(z) STF_{DA}(z)}. \quad (8)$$

Under the conditions of oversampling, $f_{lp} > f_0$ and $f < f_0 < f_s$, $LP(z)$, $STF(z)$ and $STF_{DA}(z)$ can be approximated by 1, where f_0 is the signal bandwidth. The transfer function for optimum predictor $DP(z)$ is given in (4). The digital prediction filter is simplified by using $h_1 = 1$, because calculated values for h_1 are very close to unity. This keeps the word length *BIT* in the digital part small, and $DP(z)$ becomes an ideal integrator.

C. $\Sigma\Delta$ -A/D-Converter

The signal transfer function $STF(z)$ of the $\Sigma\Delta$ -A/D-converter is [1]

$$STF(z) = \frac{1}{8z^2 - 14z + 7}. \quad (9)$$

D. $\Sigma\Delta$ -D/A-Converter

A 1^{st} -order $\Sigma\Delta$ -D/A-converter with a multi-bit internal D/A-converter with $BIT_{DA} = 12$ bits is used. Fig. 5 shows the structure of the multi-bit $\Sigma\Delta$ -D/A-converter. Because the system is already working at oversampling frequency, an interpolation-filter is not needed. The signal transfer function

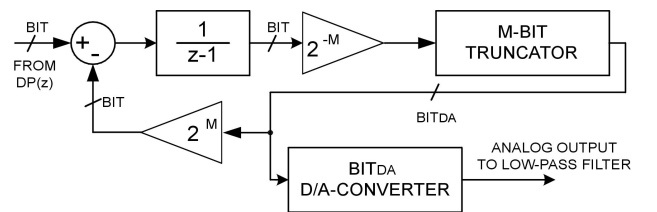


Fig. 5: 1^{st} -order multi-bit $\Sigma\Delta$ -D/A-converter.

$STF'_{DA}(z)$ of the implemented $\Sigma\Delta$ -D/A-modulator is determined as

$$STF'_{DA}(z) = \frac{2^{-M}}{z}, \quad (10)$$

where $M = (BIT - BIT_{DA})$. It deviates from the theoretical function $STF(z) = 1/z$ of Fig. 4, because the constant amplification of δ/γ is implemented for the most part by bit-shifting of M bits in the digital gain block in the forward path of Fig. 5. The residual amplification, which cannot be acquired by bit-shifting, is in the range close to unity and easily achievable in the input amplifier. The $\Sigma\Delta$ -D/A-converter is followed by the same low-pass filter $LP(z)$ as in the forward path of the encoder.

E. Encoder

According to Fig. 4, the transfer function of the whole encoder $E(z)$ is determined as

$$E(z) = \frac{U(z)}{X(z)} = \frac{\gamma STF(z)}{1 + \delta DP(z) LP(z)^2 STF(z) STF_{DA}(z)}. \quad (11)$$

F. Decoder

In order to reconstruct the input signal, a decoder $DEC(z)$ is needed. The decoder is determined as the inverse of the encoder's transfer function:

$$\begin{aligned} DEC(z) &= E^{-1}(z) \\ &= \frac{1 + \delta DP(z) STF(z) LP(z)^2 STF_{DA}(z)}{\gamma STF(z)}. \end{aligned} \quad (12)$$

The problem that $DEC(z)$ is not causal is cured in the process of combining $DEC(z)$ with a subsequent 4th-order low-pass decimation filter.

V. DIMENSIONING

In this section, the design parameters are determined such that the system requirements concerning noise and stability are satisfied.

A. Noise

The dominating noise sources are the quantization noise sources in the 1-bit $\Sigma\Delta$ -A/D-converter and in the 12-bit $\Sigma\Delta$ -D/A-modulator. The power of the quantization noise for the 2nd-order $\Sigma\Delta$ -A/D-modulator is

$$\sigma_{AD}^2 = \frac{Q^2}{12} \quad (13)$$

with the quantization step width of Q of the 1-bit quantizer of the $\Sigma\Delta$ -A/D-modulator. The 1st-order $\Sigma\Delta$ -D/A-modulator in the feedback loop creates bit-shifting (truncation) noise [5] with power equal to

$$\sigma_{DA}^2 = \frac{2^{-2M}}{12}. \quad (14)$$

In the system model, these noise sources are filtered by the corresponding noise transfer functions of the $\Sigma\Delta$ -modulators and added at the output of the $\Sigma\Delta$ -modulators.

B. Stability

For stability we consider the transfer function of the open loop

$$G(z) = \delta STF(z) STF_{DA}(z) LP(z)^2 DP(z), \quad (15)$$

which should have a phase-margin PM of more than 60° at the transit frequency, i.e.

$$PM = \arg(G(z_t)) + 180^\circ > 60^\circ, \quad (16)$$

where z_t is defined by

$$|G(z_t)| = 1. \quad (17)$$

C. Signal-to-Noise Ratio (SNR)

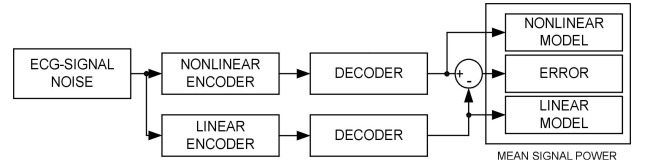


Fig. 6: SNR calculation of the simulated encoder system.

The SNR of the system is calculated from the average power at the output of the decoder $DEC(z)$

$$SNR = 10 \log_{10} \frac{\sigma_y^2}{\sigma_r^2}, \quad (18)$$

where σ_y^2 is the reconstructed signal without quantizer and σ_r^2 is the difference signal between an encoder with and without quantization, see Fig. 6.

D. Dimensioning Process

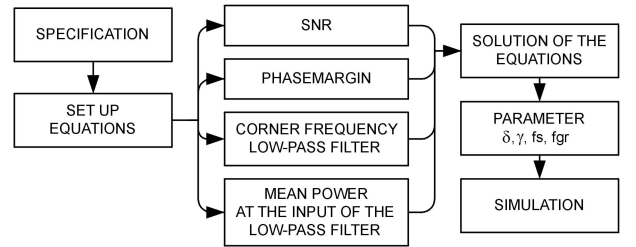


Fig. 7: Flowchart of the dimensioning process.

In order to dimension the encoder, four equations with four free parameters must be solved. The free parameters are the sampling frequency f_s , the corner frequency of the low-pass filter f_{lp} , and the factors δ and γ . The four equations are: i) a restriction of the mean power in the forward path in order to avoid overloading of the $\Sigma\Delta$ -A/D-modulator; ii) the corner frequency f_{lp} of the low-pass filter (5); iii) the signal-to-noise ratio SNR (18); iv) the phase-margin PM (16). Then, for a given set of specifications, the equations are solved numerically with MathCAD. Fig. 7 shows a flowchart for the dimensioning process.

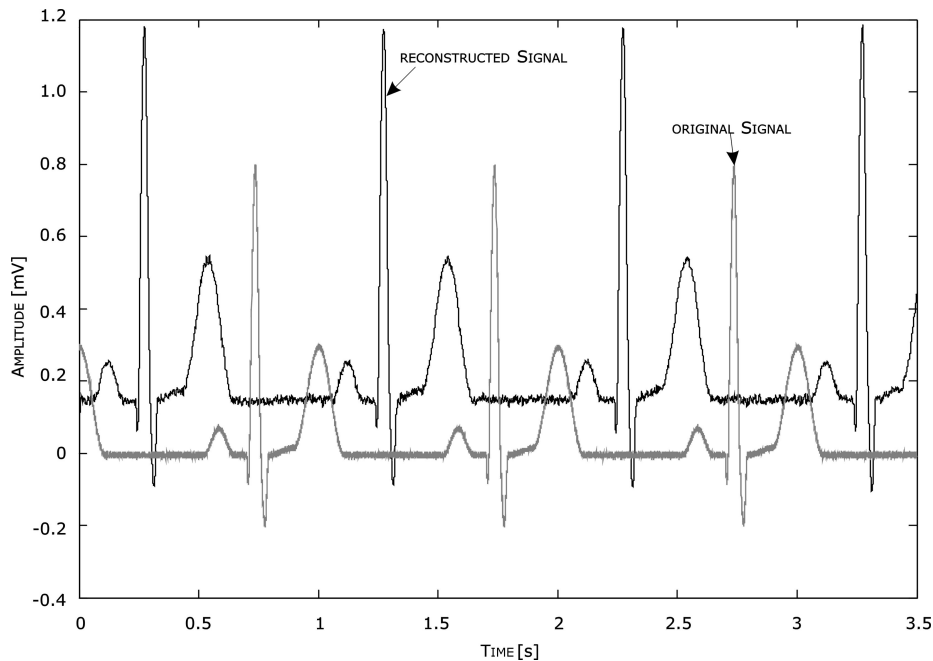


Fig. 8: Original and reconstructed ECG-Signal obtained from the prototyped circuit.

VI. SIMULATION RESULTS

After the parameters for an optimum converter with respect to specifications have been found, they are extracted from MathCAD and used to simulate the system in Matlab/Simulink. Simulink can simulate the encoder-system in transient time, and all nonlinear effects like saturation within the analogue front-end and quantization noise from the $\Sigma\Delta$ -modulators are considered in the simulation model. In Table I, the used specifications for the SNR , PM and Q as well as the derived parameters are shown. The word length BIT results from the desired DC-offset at the input amplifier. With respect to the conventional channel, a significant reduction of the sampling frequency can be accomplished, which can also be translated to power savings in the $\Sigma\Delta$ -A/D-Modulator. Besides, as mentioned in Sec. II, a larger gain γ in the input amplifier can be exerted.

TABLE I: Parameter for the ECG-encoder.

Specification / Parameter	conventional ECG-Channel	ECG with prediction [1]	ECG with digital prediction
SNR	72 dB	72 dB	60 dB
PM	$> 60^\circ$	$> 60^\circ$	$> 78^\circ$
Q	1.65 V	1.65 V	1.65 V
$DC\text{-Offset}$	± 0.3 V	± 1 V	± 1.2 V
f_s	250 kHz	39.5 kHz	34 kHz
γ	20	2314	1189
δ	-	0.0378	0.27
BIT	-	-	19 bits

VII. REALIZATION OF THE ENCODER AS A PROTOTYPE

The system has been prototyped on a PCB using the integrated analogue front-end of [2], an FPGA and a discrete D/A-

converter. The FPGA has been used for the whole digital part in the feedback loop with a synchronized clock input from the $\Sigma\Delta$ -A/D-converter. The SNR was determined experimentally by digitizing the output of the $\Sigma\Delta$ -A/D-converter and using a software decoder programmed in Matlab/Simulink. Fig. 8 shows the input signal and the reconstructed output signal. A SNR value of 35 dB was measured, which is close to the average experimental value of 40 dB reported in [1]. Compared to the simulated value of 60 dB, the realized system was subjected to environment noise and noise caused by external components. The system showed excellent stability behaviour. Even dramatic DC-offsets of up to ± 1.2 V could be sustained without becoming unstable.

VIII. CONCLUSION

The concept for using a digital prediction filter is fully synthesizable on chip. Advantages of the predictive converter include the processing of ECG signals with DC-offsets up to ± 1.2 V around analogue ground and the reduction of the sampling frequency. Because the feedback loop is mostly digital, the impact of noise is reduced significantly with respect to an analog predictor in a previous implementation. Compared to the standard open-loop system for processing ECG-signals (cf. Fig. 1), the new system consumes about 50% less power in the $\Sigma\Delta$ -A/D-modulator.

REFERENCES

- [1] B. Fuchs: *Integrierte Sensorschaltungen zur EKG- und EEG-Ableitung mit prädiktiver Signalverarbeitung*. Ph. D. Dissertation, TU Hamburg-Harburg, Shaker-Verlag, 2004.
- [2] C. Bronskowski: *A Programmable Analog Front End for the Acquisition of Biomedical Signals*. ProRISC2004 Workshop, 2004, pp. 474-477
- [3] R. Steele: *Delta Modulation Systems*. Pentec Press London, 1975
- [4] C. Zywiets: *ECG-CTS-Test-Atlas*. Biosignalverarb. MH-Hannover, 1991
- [5] A. V. Oppenheim, R. W. Schaffer: *Discrete-time signal processing*. Upper Saddle River NJ, 1999