Non Volatile Memory Cells integrable using standard CMOS Processes

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Abstract— **Two non-volatile memories compatible with CMOS processes in 0.35 µm technology are studied and compared. The PMOS version of the cell is presented and compared with its NMOS counterpart. Hot hole injection is studied as an altenative to Fowler Nordheim tunneling to decrease the operating voltages. Measurement results are presented and discussed.**

Keywords—**Non-volatile memory; CMOS compatible; single poly, hot-hole injection.**

I. INTRODUCTION

Non-volatile memories compatible with CMOS processes may provide a way to decrease the cost of system on chip and ASIC integrated circuits and at the same time, eases the integration process of system on chip ICs. With this kind of memory cells, virtually anyone having access to a standard CMOS process may be able to incorporate small memories into an IC.

In addition to this, lower programming and erasing voltages are required for battery-powered and mobile applications. Lowering the programming voltages also reduces the chip area required for charge pumps, which usually require much silicon area due to the size of the pumping capacitors.

In this work, two CMOS compatible memory cells are studied and compared. The memory cell presented in [1] and its PMOS counterpart were fabricated using 0.35µm technology. The NMOS cells were programmed by hot hole injection and erased by hot electron injection. The PMOS cells were programmed by hot electron injection. These operating mechanisms proved to require low bias voltages and to be an effective way to operate the cells

II. HOT CARRIER INJECTION

The programming and erasing operations of the cells are based in hot carrier injection. For the NMOS, the programing mechanism is the hot hole injection, while erasing is performed by hot electron injection. For the PMOS, the programing mechanism is the hot electron injection, while erasing is performed by hot hole

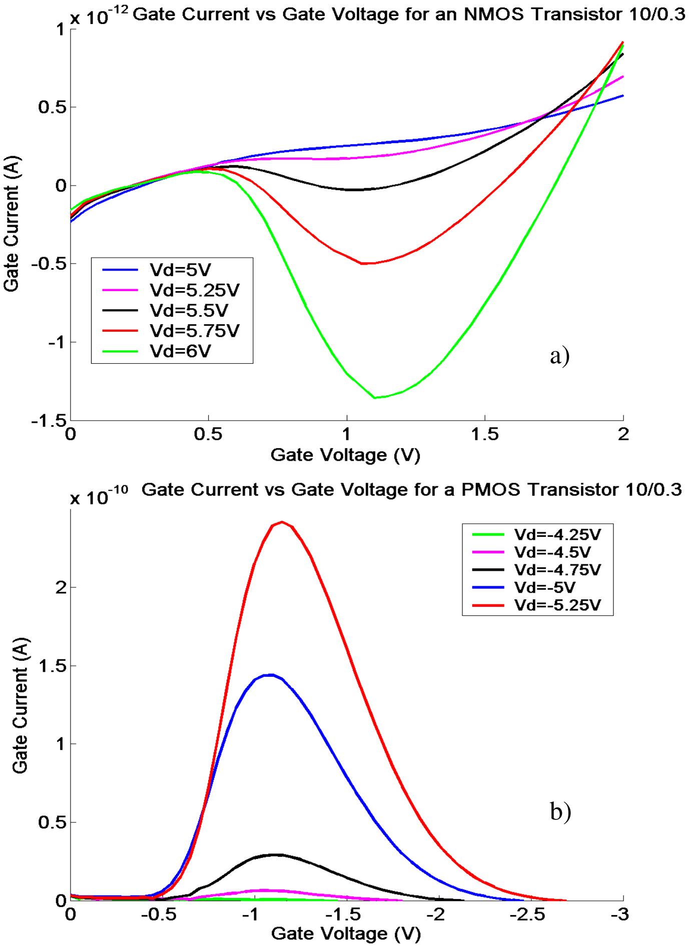

Figure 1. a) Hot hole injection in NMOS
b) Hot electron injection for PMOS

injection. In order to obtain the bias parameters to perform hot carrier injection programming for the memory cells, the gate current of single transistors was measured.

Figure 1 shows the hot hole current obtained for a NMOS transistor in 0.35µm technology for the transistor dimensions 10µm /0.3µm . Similarly, the gate current of PMOS transistors was measured to determine the conditions for hot electron injection. Figure 2 shows the hot electron current for a PMOS transistor in 0.35µm technology for the transistor dimensions 10µm /0.3µm.

From this, it can be concluded that the PMOS transistor has a much better efficiency for injection in the low voltage range, since electrons have a higher injection efficiency than holes and the PMOS transistor in this measurement is a buried device[3]. Compared to the NMOS, the conditions for the magnitude of the gate voltage are similar in both cases. However, hot carrier injection can be first measured at a drain voltage Vd of -4V for the PMOS transistor, whereas hot carrier injection starts at 5.25V for the NMOS transistor.

For both the PMOS and NMOS transistors, the peak of hot carrier injection current in the low gate voltage regime is measured at a gate voltage of about 1V. This favours the cell operation, since low voltage needs to be coupled to the floating gate in order to program the cells.

II. BASIC CELL STRUCTURE

The cells, fabricated in 0.35 µm technology, consist of an access transistor connected to a floating gate transistor. The access and floating gate transistors are of the same type, therefore saving cell area as compared to previous approaches, like the SIPPOS cell[1].

The schematics presented on figure 2 shows the cell configuration for both the NMOS and PMOS cells.

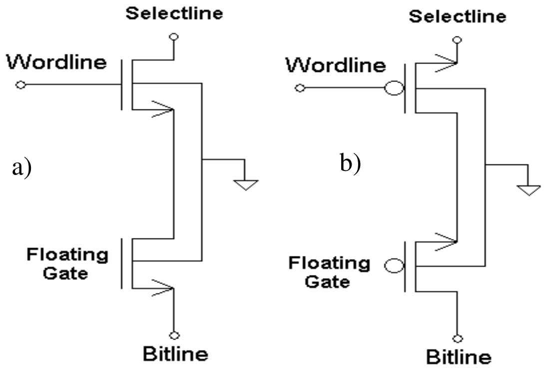

Figure 2. Schematics of the measured cells:
a) NMOS cell after [1], b) PMOS cell

For the reading operation, the wordline and selectline area biased, whereas the bitline is grounded. For the program and erase operations, the wordline and bitline are biased and the selectline is grounded.

III. CELL READING

As mentioned before, the cell is read by biasing the wordline and selectline and grounding the bitline. Figure 3 shows the cell characteristics for increasing selectline voltage at different wordline bias conditions.

From figure 3 it can be observed that the PMOS cell requires lower wordline and selectline voltages for the reading operation, making it a better option than the NMOS cell for low voltage operation.

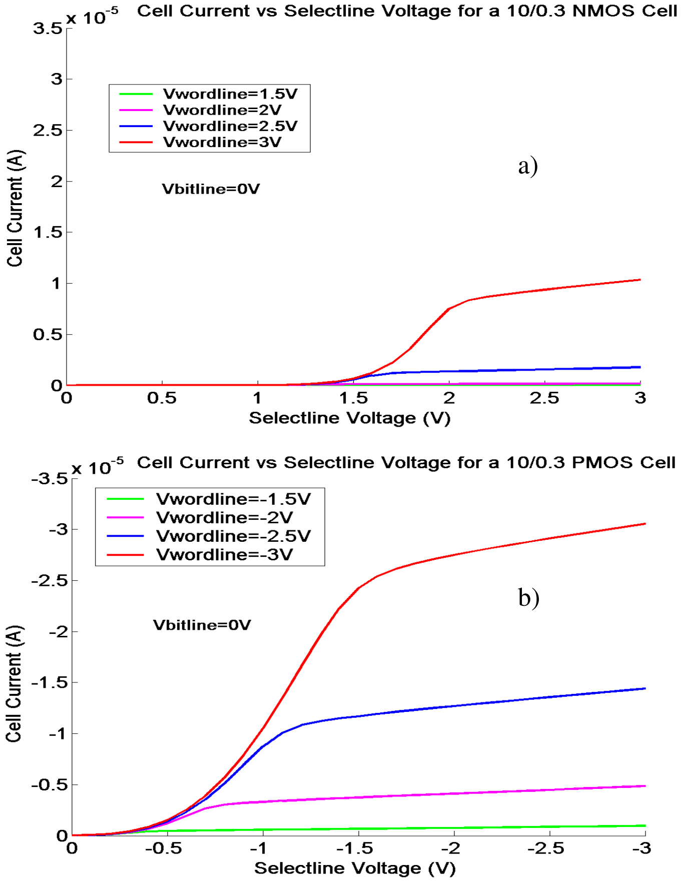

Figure 3. Cell reading characteristics
a) Cell Current, NMOS cell
b) Cell Current, PMOS cell

IV. CELL PROGRAMMING

The required bitline voltage for the programming operation was determined from the measurement of single transistors. The programming mechanism for NMOS cells is hot hole injection, whereas hot electron injection is the programming mechanism for PMOS cells.

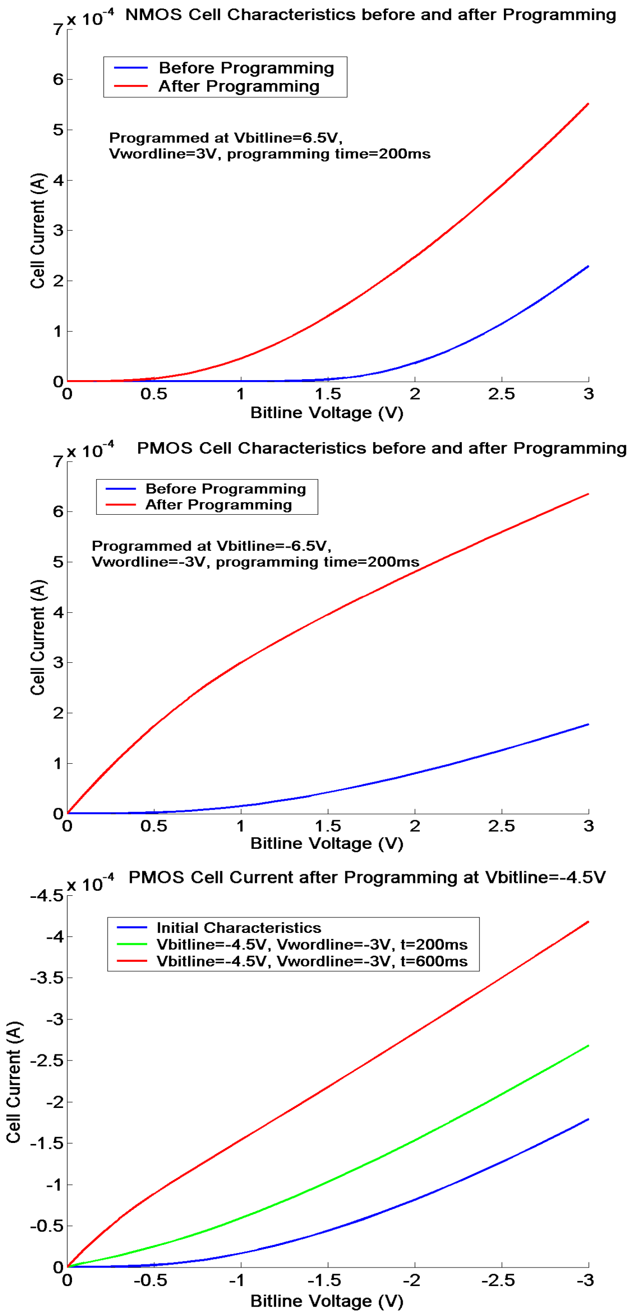

Figure 4. PMOS and NMOS cell characteristics before and after programming.

It was determined that the PMOS cell can be programmed with bitline voltages as low as –4.5V, as shown in figure 4. The bitline and selectline characteristics before and after programming for $|V_{wordline}|=3V$, $|V_{bitline}|=0..3V$ and grounded selectline are presented in figure 4.

In case of the NMOS cell, the minimum programming voltage was 6V. Bitline voltages lower than 6V lead only to degradation of the series resistance, but caused no shift in the cell's threshold voltage.

Figure 4 also shows the bitline current before and after programming at $|V_{bitline}|=6.5V$, $|V_{wordline}|=3V$ for a programming time of 200ms. The characteristics for both PMOS and NMOS were measured with the bitline voltage varying from $|V_{bitline}|=0..3V$, $|V_{wordline}|=3V$ and grounded selectline.

From this table it can be observed that the cell with the longest distance between the gates presented the highest increase in bitline and selectline currents, although it presented the lowest bitline and selectline currents before the programming operation. This suggests that the longest separation between gates provides the best field conditions for programming, since the proximity of the gates increases the poly to poly coupling factor and the voltage in the node conecting the access and the floating gate transistor.

Table 1. Comparison of cell currents before and after programming at $|V_{wordline}|=3V$, $|V_{bitline}|=6.5V$ during 200ms.

a) for the bitline at $|V_{wordline}|=3V$, $|V_{bitline}|=3V$,
b) for the selectline at $|V_{wordline}|=3V$, $|V_{selectline}|=3V$.

	Cell01	Cell02	Cell03	PMOS
$|I_{bitline}|$ before (µA)	229	370	55	178
$|I_{bitline}|$ after (µA)	552	557	494	635
Increase factor	2.41	1.45	8.94	3.58
$|I_{selectline}|$ before (µA)	10	61	0.48	30.6
$|I_{selectline}|$ after (µA)	148	146	205	359
Increase factor	14.3	2.41	425	11.7

It can also be observed that even when the PMOS transconductance is 2.93 times lower than that of the NMOS and the magnitude of its threshold voltage is 150mV higher, it presents a higher increase of the bitline current than the NMOS cell, under the same voltage, time and gate separation conditions. The increase factor of the selectline current is also on the same order of magnitude than that of the NMOS cell 1. This confirms the higher efficiency of hot electron injection on these transistors.

These observations and the influence of the gate separation suggest that optimization of the PMOS cell may increase its efficiency for programming at a bitline voltage of –4.5V, therefore favoring low voltage operation. This optimization should also shorten the programming times to achieve acceptable performance. However, under higher bias conditions, the PMOS cell decreases its threshold voltage excesively, in comparison to the NMOS counterparts

V. CELL ERASING

Unprogrammed, virgin cells were biased for the same erase conditions in order to compare the erase efficiency for each case. The erasing mechanism for NMOS cells is hot electron injection, whereas the erasing mechanism for PMOS cells is hot hole injection.

The main results of these comparison are summarized in table 2. The cells were biased at $|V_{wordline}|=1$ V, $|V_{bitline}|=6.5$V, $|V_{selectline}|=0$V during 200ms. For the same bias conditions, the PMOS cell showed no change either in the cell current, neither in the threshold voltage. On the other hand, the NMOS cell of type 1 presented negligible shift of the threshold voltage. The decrease in the cell current is mainly due to degradation of the series resistance.

The NMOS cell type 2 presented an increase in the threshold voltage. This cell presented the most efficient erasing, as shown in figure 6. On the contrary, the NMOS cell type 3 decreased its threshold voltage, therefore verifying that the minor influence of the wordline coupling is an effective way to inject holes but makes more difficult to couple the required voltage magnitude for hot electron injection. However, it was possible to erase previously programmed cells at this bias. This was confirmed for the NMOS cells type 1 and 2, as shown in table 3.

For the same magnitudes of voltage bias for the PMOS cell, no threshold voltage shift was observed. However, at $|V_{wordline}|=1.5$V, $|V_{bitline}|=6.5$V, $|V_{selectline}|=0$V during 200ms, hot electron injection was possible. This leads to cell programming rather than cell erasing. The reason for that can be explained with help of figure 2b. The higher the bitline voltage, the higher the voltage coupled to the floating gate. However, the higher bitline voltage also leads to a wider hot electron injection curve. This means, even by coupling higher voltages to the floating gate, the transistor is still operating in the hot electron injection regime. This situation gets worse after the programming operation, since the higher cell current means that more carriers can be heated and injected.

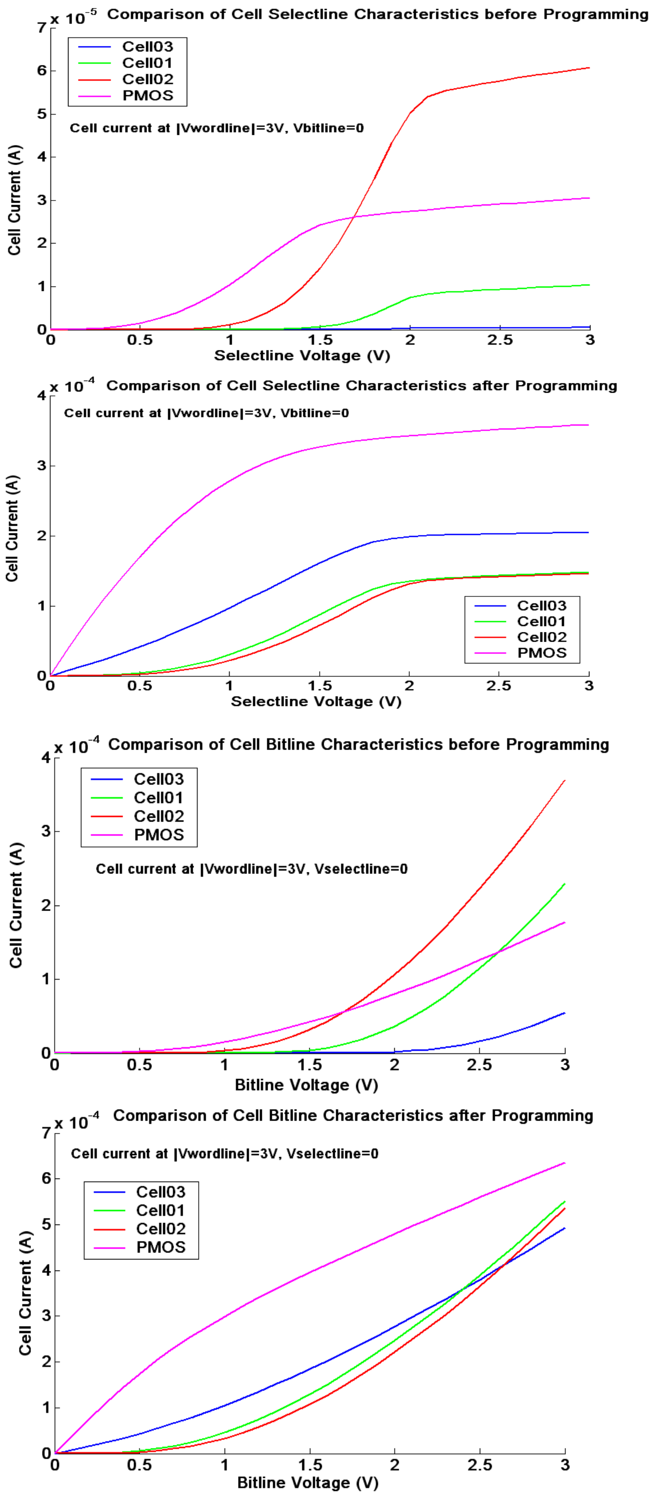

Figure 5. Comparison of cell characteristics before and after programming at $|V_{bitline}|=6.5$V, $|V_{wordline}|=3$V and 200ms programming time a) and b) as function of the bitline, c) and d) as function of the selectline

Table 2. Comparison of cell currents before and after erasing bias at $\lvert V_{wordline}\rvert$=1V, $\lvert V_{bitline}\rvert$=6.5V during 200ms

a) for the bitline at $\lvert V_{wordline}\rvert$=3V, $\lvert V_{bitline}\rvert$=3V,
b) for the selectline at $\lvert V_{wordline}\rvert$=3V, $\lvert V_{selectline}\rvert$=3V.

	Cell01	Cell02	Cell03	PMOS
$\lvert I_{bitline}\rvert$ before (µA)	150	359	39.1	169.5
$\lvert I_{bitline}\rvert$ after (µA)	128	173	125	172.3
Increase factor	0.85	0.48	3.2	1.02
$\lvert I_{selectline}\rvert$ before (µA)	3.88	71.3	0.3	26.9
$\lvert I_{selectline}\rvert$ after (µA)	1.7	5.93	8.13	26.4
Increase factor	0.438	0.083	27.1	0.98

Table 3. Comparison of cell currents for previously programmed cells before and after erasing bias at $\lvert V_{wordline}\rvert$=1V, $\lvert V_{bitline}\rvert$=6.5V during 200ms

a) for the bitline at $\lvert V_{wordline}\rvert$=3V, $\lvert V_{bitline}\rvert$=3V,
b) for the selectline at $\lvert V_{wordline}\rvert$=3V, $\lvert V_{selectline}\rvert$=3V.

	Cell01A	Cell01B	Cell02
$\lvert I_{bitline}\rvert$ before (µA)	216	317.5	405.5
$\lvert I_{bitline}\rvert$ after (µA)	95.5	103	133
Factor	0.442	0.324	0.328
$\lvert I_{selectline}\rvert$ before (µA)	8.04	43.9	88.9
$\lvert I_{selectline}\rvert$ after (µA)	0.34	0.69	1.67
Factor	0.043	0.016	0.019

VI. CONCLUSIONS

The results of this work show that the PMOS cell has the potential to operate at lower programming voltages than the NMOS cells. However up to now, cell erasure has not been observed. Nevertheless, the cell can be operated as OTP and its coupling characteristics can be optimized to make hot hole injection possible and to better control hot hole injection.

In addition to this, the importance of the proximity of the access transistor gate and the floating gate for both the programm and erase operations was presented. Optimization of this distance may also contribute to decrease the cell operating voltages and/or shorten the programming and erasing times.

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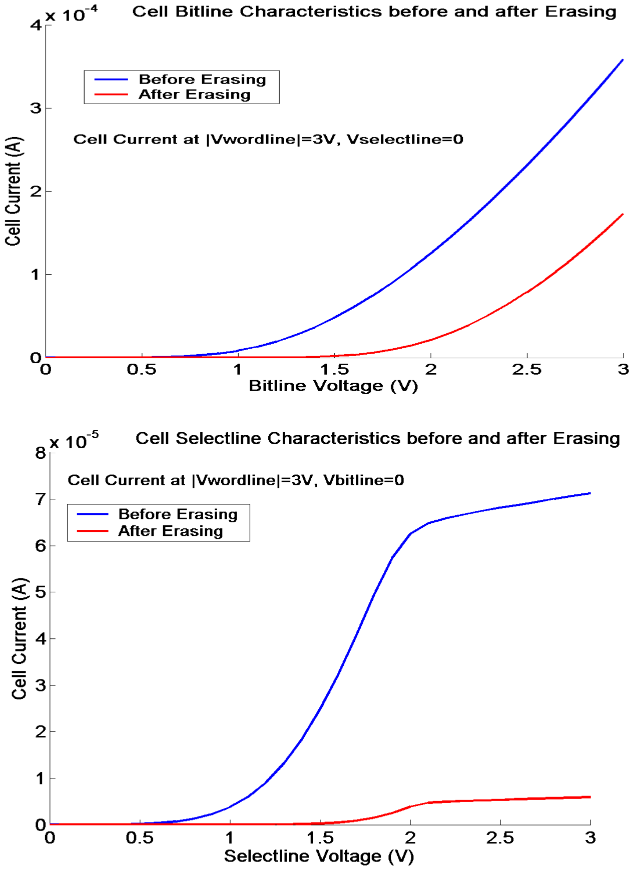

Figure 6. Comparison of cell characteristics before and after the erasing operation at $\lvert V_{bitline}\rvert$=6.5V, $\lvert V_{wordline}\rvert$=1V during 200ms
a) For the Bitline
b) For the Selectline