

Ultra High-Speed Sampling Track-and-Hold Amplifier in SiGe Bi-CMOS Technology

David Smola, Hendrik v. d. Ploeg, Maarten Vertregt, Lucien Breems, Johan Huijsing, Kofi Makinwa

Abstract—In this paper, design and simulation results of a bipolar 5GS/s track-and-hold (T&H) circuit for high-frequency applications is presented. The circuit has been designed in an advanced SiGe heterojunction Bi-CMOS technology. Due to the large bandwidth requirements the topology of such T&H is fully differential using an open-loop concept. This approach ensures good linearity performance and acceptable droop rate. The hold-mode feedthrough is compensated with an additional circuitry. The design uses only NPN transistors in order to fulfill the high-frequency specifications.

The track-and-hold design is based on a switched-emitter follower principle employing input and output buffers. The clock signals are generated off-chip and re-amplified on-chip with clock buffers. In simulations was used a model of the clock generator to see the effect of the clock jitter contribution on the overall performance.

As a performance measure is used a spurious-free dynamic-range (SFDR) analysis. For 5GHz sampling frequency, simulation results of the layout-extracted view of the designed T&H achieve SFDR close to 55dB for a 1V full-scale input sinewave signal of 1GHz.

Index Terms — track and hold, state-of-the-art, switched-emitter follower, jitter.

I. INTRODUCTION

THE current demand for high-resolution and fast analog-to-digital converters (ADC) is driving the need for track-and-hold amplifiers (T&H) operating at RF frequencies. A very fast and linear T&H circuit is the key element in any modern wideband data acquisition system. Applications like a cable-TV or a broad variety of different radio standards require high processing speeds with high resolution. Systems containing such a wideband processing blocks can replace several implemented narrowband receiver front-ends typically used in multi-band receivers. Further, the wideband solution helps to save the chip area, therefore reducing costs. Having a wideband and precise acquisition system is a prerequisite for today's trend towards multi-standard flexible radios, with as much signal processing as possible in the digital domain.

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A state-of-the-art example of a T&H amplifier in a CMOS technology is illustrated in [1]. A state-of-the-art example in a Bi-CMOS technology realization is described in [2] or [3]. Both realizations exceed sampling rates of 1 GS/s and achieve spurious free dynamic range (SFDR) above 50dB.

This paper presents a design of a track-and-hold circuit in a Bi-CMOS process achieving simulated SFDR up to 55dB and sampling rates up to 5GS/s. The design is intended for a general usage in state-of-the-art multi-standard high data-rate systems e.g. base-station applications or laboratory instrumentation.

II. ARCHITECTURE

A. The principle

The architecture of a T&H should allow the circuit to be very wideband with an extremely fast response to an input signal. Therefore, the current structure uses the differential open-loop approach. The principle of the T&H is illustrated in Figure 1 (only a single-ended signal path is depicted).

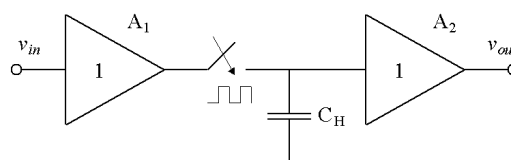


Fig. 1. Block schematic of a single-ended track and hold system.

The input signal is buffered via A_1 before being sampled by the sampling switch. The signal stored at the hold capacitor C_H is buffered to the output via A_2 . To achieve very high sampling rates, the switching as well as the buffering transistors are bipolar. But since the structure is an open-loop topology, parasitic effects of the transistors are not reduced, as it would be in a system containing certain negative feedback. Therefore, the non-idealities of the topology are reduced with additional compensation: the feedthrough due to the bipolar transistors is minimized with a feed-forward compensation; the common-mode effects are eliminated with the differential mode of operation.

Principle of the bipolar open-loop track-and-hold circuit is illustrated in Figure 2 (single-ended signal path). The topology is known as a switched emitter follower [4]. The switch is formed by a single bipolar transistor Q_{switch} . It is in an on-state (tracking) if the biasing current I_2 is on and I_1 is off. When the currents are switched in a complementary way,

I_1 conducts and I_2 is off, the circuit is in an off-state (holding).

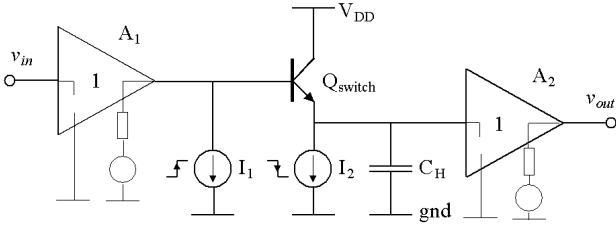


Fig. 2. The switched emitter follower principle.

The main purpose of the biasing current I_1 is to pull down the voltage at the base of Q_{switch} such that the transistor is biased in the cut-off region of operation. In an ideal case, the voltage on C_H would then remain constant until the transistor is switched to an on-state again. Usage of the complementary biasing current I_1 and pull down of the base voltage is necessary due to the fact that the “threshold” voltage V_{be} of Q_{switch} is rather high, close to 1V. The high V_{be} is because the transistor contains within its active area Germanium dopants.

B. Non-idealities

There is a broad variety of errors limiting the T&H performance, generally split into two groups: timing-related errors and amplitude-related errors.

The timing-related errors appear mainly due to the oscillator imperfections. The oscillator output frequency is not exact but varies during the time. It is expressed by a quantity so-called phase noise. It greatly affects the sampling precision. The phase noise is often expressed in terms of a timing jitter [5].

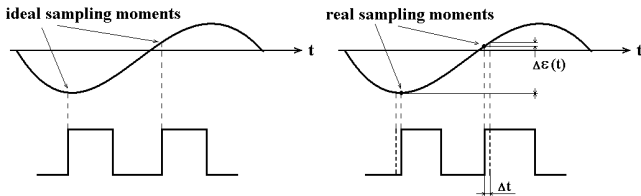


Fig. 3. The effect of timing uncertainty on sampling.

The effect of timing uncertainty on the sampled signal uncertainty is shown in Figure 3. The time error i.e. the phase error is marked with Δt and its consequence is the error that appears in the sampled value, named as $\Delta \epsilon(t)$. The amplitude error is a critical measure for a design of any T&H and is related to the phase error, which is critical measure in an oscillator design. The effect of a timing-related error is expressed in Signal-to-Noise Ratio (SNR). For a sinewave input signal the mathematical relation among the quantities is:

$$SNR_{dB} = -20 \log(\omega \cdot \Delta t_{rms}) \quad (1)$$

where ω is the angular frequency of the input signal and term Δt_{rms} is the RMS quantity of the time error Δt (so called jitter). For example to achieve at least 60dB of SNR for 1GHz signal the timing error should be as small as 0.16ps. It is already in a range of nowadays state-of-the-art oscillator designs [6].

The main amplitude-related error in the design of any track-and-hold circuit in a bipolar technology is so-called

feedthrough. It originates from the actual presence of the intrinsic B-E capacitance of the switch transistor. Therefore in the hold mode the base of the transistor Q_{switch} presents certain final impedance for the input signal.

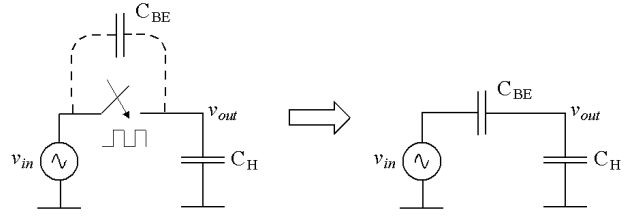


Fig. 4. Illustration of the feedthrough mechanism in the hold mode.

In Figure 4, there is shown the mechanism of the feedthrough effect. The hold capacitor C_H and the base-emitter capacitance C_{BE} form a capacitive divider. When the input signal is a sine wave, the highest amplitude error in the hold mode appears for the highest slope of the signal. To ensure the amplitude error is within defined fraction of the actual signal amplitude, condition (2) is derived.

$$error < \frac{T_{sample}}{2} \frac{C_{BE}}{C_{BE} + C_H} A \cdot 2\pi \cdot f_{signal} \quad (2)$$

E.g. if the amplitude error due to the feedthrough is to be 50dB lower than the full signal swing, for 1V peak-peak sine wave the error should be smaller than 3mV. With capacitance C_{BE} of a cut-off biased transistor of 10fF and with 1GHz input signal and 5GHz sampling rate, the hold capacitor C_H must be bigger than 1pF. It is a tight requirement with respect to the required bandwidth (step response). Lowering the switching transistor size can reduce the feedthrough effect, but it has also certain limits. Therefore the hold capacitor C_H is selected with lower capacitance and the existing feedthrough is minimized by a proper compensation.

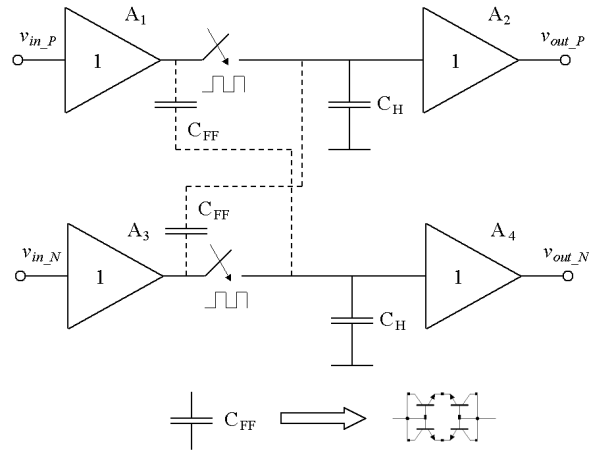


Fig. 5. The feedthrough compensation, top is the principle, bottom is the compensation capacitor realization.

The feedthrough compensation principle is depicted in Figure 5. Because of the differential operation, in the hold mode the charge stored at a compensation capacitor C_{FF} is of opposite sign than the charge stored at the hold capacitor C_H . If both capacitors are equal, the compensation is ideally

perfect. This is further illustrated mathematically with equation (3) for the feedthrough transfer function H_{FF} [4].

$$H_{FF} = \frac{C_{BE}}{C_{BE} + C_H} \left(1 - \frac{C_{FF}}{C_{BE}} \right) \quad (3)$$

The aim is to have the compensation capacitor C_{FF} as similar as possible to the base-emitter capacitor C_{BE} of the switching transistor. In [4] there is suggested the topology of the compensation capacitor, shown in Figure 5 at the bottom.

III. CIRCUIT DESIGN

A fully differential representation of the track-and-hold circuit is shown in Figure 6. The circuit is designed only with NPN transistors, poly-resistors and poly-capacitors, available in the technology. The MOS devices of the process were used only as decoupling capacitors.

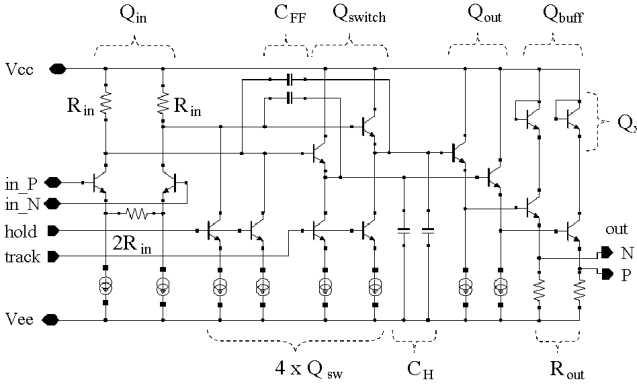


Fig. 6. The full circuit schematic of the T&H.

A. Circuit description

The schematic can be divided into four blocks. The input buffer is built from two identical transistors Q_{in} and load resistors R_{in} connected in a degenerated differential pair. Such that the buffer exhibits gain close to unity.

The differential switch is formed by two identical transistors Q_{switch} , two pairs of complementary-clocked transistors Q_{sw} , hold capacitors C_H , and the feedthrough compensation capacitors C_{FF} .

The output buffer includes two sensing transistors Q_{out} , two buffering transistors Q_{buff} biased by resistors R_{out} .

The track-and-hold is biased by a matched net of local current sources. The two transistors Q_x connected at the collectors of transistors Q_{buff} are placed for protective reasons against high voltage spikes during switching the T&H circuit on/off.

When the node “track” is on logic H the Q_{switch} transistors are in a forward-active mode acting as emitter followers, thus tracking the input signal. When the node “hold” changes to a logic H, the Q_{switch} transistors go to an off mode. The proper pair of the Q_{sw} transistors starts to withdraw the current from resistors R_{in} leading to a voltage pull-down at the base of both Q_{switch} transistors, ensuring both Q_{switch} are correctly off. The signal stored in the hold capacitors C_H is sensed by transistors Q_{out} that are biased for high β_F . Such that the base current is

minimized so is the voltage drop in the hold mode across C_H . To buffer the signal to a low-ohmic/high capacitive load the buffering transistors Q_{buff} form a quasi-differential emitter follower, characteristic for its low output impedance across a very wide range of frequencies.

One of the most stringent parameter within the design is the value of the hold capacitor C_H . It should fulfill requirements with respect to the feedthrough, to the thermal noise (“ kT/C ” noise) and to the bandwidth of the system. The switch has to be fast enough for a step response to settle within a fraction of the sampling period. Referring to Figure 2 the switch is formed by the switch transistor Q_{switch} , by a biasing current I_2 and by a holding capacitor C_H . The current-voltage relationship of the capacitor can be expressed as

$$v_C(t) = \int \frac{1}{C_H} \cdot i dt \quad (4)$$

where $v_C(t)$ is the voltage at the emitter of Q_{switch} and $i(t)$ is the instantaneous value of the biasing current I_2 . For the most extreme case of transition the complete current I_2 is supplied and the transition is across the full single-ended swing. If the signal swing V_{pp} is 0.5V and the wanted time to settle τ_F is 25% of the sampling period of a 5GHz sampling rate, then $C_H < \tau_F \cdot I_2 / V_{pp}$ and for the hold capacitance C_H of 400fF the minimal biasing current of 4mA is required.

B. The clock signals

As was described in the section II the performance of the overall track-and-hold circuit depends upon the quality of the clock signal. For the simulations a model of a clock circuit was created using language Verilog A. The block schematic of the model is in Figure 7.

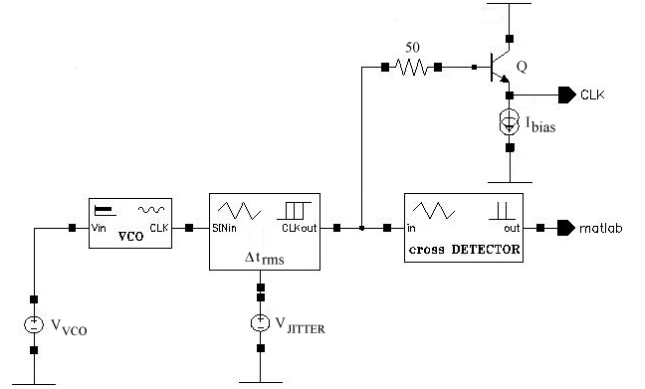


Fig. 7. A single-ended model of a clock circuit with programmable jitter.

The VCO is driven by a DC voltage V_{VCO} , setting its current oscillating frequency. The subsequent block is basically a comparator with programmable jitter. The RMS quantity of the jitter is set by a DC voltage V_{JITTER} . The clock signal in proper voltage level is then fed via 50Ω resistor into the clock buffer. The buffer is formed by a transistor and a biasing current source. They together form an emitter follower with low output impedance capable to drive the switching transistors inside the T&H. The cross detector senses the zero crossing positions of the jittered signal. Matlab then can be

used to see the effect of the clock jitter on the actual performance of the T&H. For simulation purposes of the design presented in this paper the amount of jitter injected into the clock signal was set to 0.15ps. In state-of-the-art oscillator designs there have already been achieved values as low as that, illustrated for example in [6].

IV. LAYOUT

The layout of the designed track-and-hold is shown in Figure 8.

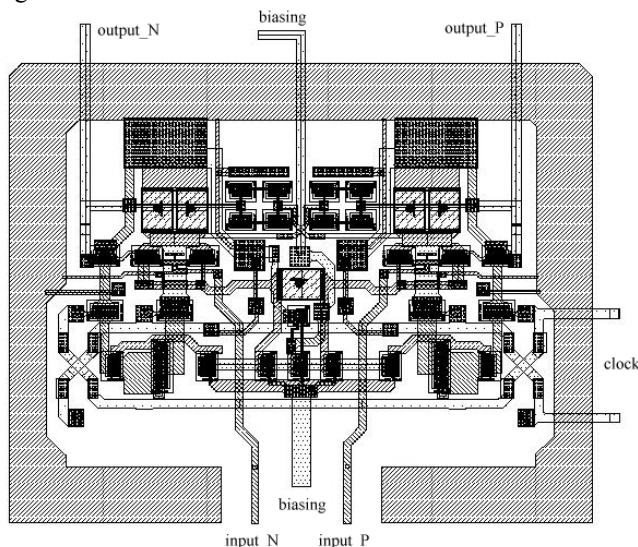


Fig. 8. The full circuit layout of the T&H.

The technology uses 6 metal layers. The circuit is encapsulated in an M1 ring with substrate connections to reduce a crosstalk from the neighboring circuitry (clock, digital logic etc). The layout is symmetrical with the biasing line as the axe of symmetry. The loading resistors R_m are in a parallel connection in order to split the current so that the electromigration limits of the poly-layer are not exceeded. In between the loading resistors are the matched transistors as the C_{FF} capacitor for the feedthrough compensation. Layout of the signal lines versus the clock lines is perpendicular to minimize the crosstalk. Also the clock signal uses the upper metal layer. All the circuitry is layouted such that the differential signals (input, clock) see a symmetrical load.

V. SIMULATION RESULTS

The T&H was designed for sampling frequencies up to 5GHz. All the presented results are taken from simulations. For simulations was used the layout-extracted circuit of the T&H. All signals were differential. The input sinewave signal, 1V peak-peak differentially, was simulated with an ideal source with 50 Ω series resistance. The sampling frequency was 5GHz and the extra-injected jitter into the clock signal was in the order of 0.15ps. In Figure 9, there is a plot of the selected performance measures versus the input signal frequency. The measures were taken from the FFT analysis of the differential output sampled signal.

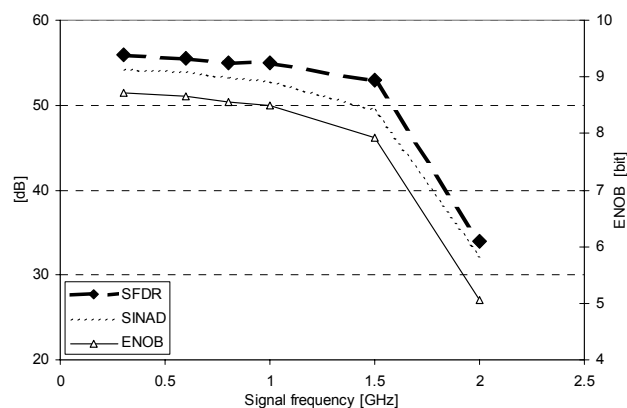


Fig. 9. Simulated SFDR, total SINAD and ENOB of the T&H for different input frequencies. Sampling frequency 5GHz.

SFDR was specified as the power difference between the signal and its third harmonic. The Signal-to-Noise And Distortion (SINAD) ratio illustrates the total contribution of all calculated higher harmonic spurs to the final SNR. From this quantity it is derived the total Effective Number Of Bits (ENOB) for an eventual comparison with other designs.

Simulations show that the sampled signal exhibits maximally 0.9mV/100ps droop rate at the output of the T&H. The power consumption of the T&H itself is 240mW.

VI. CONCLUSIONS

This paper presents a design of a wideband track-and-hold circuit in SiGe Bi-CMOS process. According to simulations of the layout-extracted view the circuit achieves 55dB of SFDR for a sampling rate of 5.0GHz and for 1GHz input sinewave signal. The power consumption of the T&H with no auxiliary circuitry is 240mW.

VII. ACKNOWLEDGEMENTS

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