

# Downconversion Schemes for a mm-Wave CMOS Receiver for Short Range Gigabit Communication

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**Abstract**—The heterodyne receiver is a favored architecture for a mm-wave receiver design. It eases the demands on the noise and gain performance of the preamplifier. This system operates with a lower frequency local oscillator (LO), which saves current compared to a homodyne receiver, and allows a conventional voltage controlled oscillator (VCO) design. Furthermore, the quadrature phases needed for the filtering and demodulation can be generated without an extra circuitry such as a poly-phase filter.

To sidestep the necessity of an additional LO source, a sliding intermediate frequency (IF) scheme is used. A major difficulty in the implementation of this architecture is the leakage of higher order harmonic products into the baseband. In this paper a comparison is performed between two frequency schemes,  $F_{LO} = \frac{2}{3}F_{RF}$  and  $F_{LO} = \frac{4}{5}F_{RF}$ . From this analysis the specifications of the interstage filter are derived. The circuits are simulated in 65nm/90nm CMOS process.

## I. INTRODUCTION

Continued scaling of CMOS technology allows RFIC designers to exploit the unlicensed 7GHz of free spectrum around 60GHz. The proposed 802.15.3c standard for short-range, gigabit/s communication in the unlicensed bands at 60GHz may be used as an adapter for any gigabit/s data source or sink requiring a short-range wireless link. The spectral allocations vary with region as shown in the following table.

TABLE I: Unlicensed Bands

Region	Unlicensed Band
USA	57 – 64 GHz
Europe and Japan	59 – 66 GHz

The small physical size of passive circuit elements at mm-wave frequencies enables more cost-effective integration of distributed elements such as antennas or baluns. A second benefit of mm-wave operation is immunity to interference due to attenuation (see Fig. 1) of the transmitted signal at 60GHz caused by absorption of the RF energy by oxygen ( $O_2$ ). This natural immunity to interferers can relax the demand on the front-end circuit linearity, thereby conserving current and power consumption. Early demonstrations of 60GHz communication transceivers used silicon bipolar devices in an advanced BiCMOS technology [2], [3]. However, CMOS

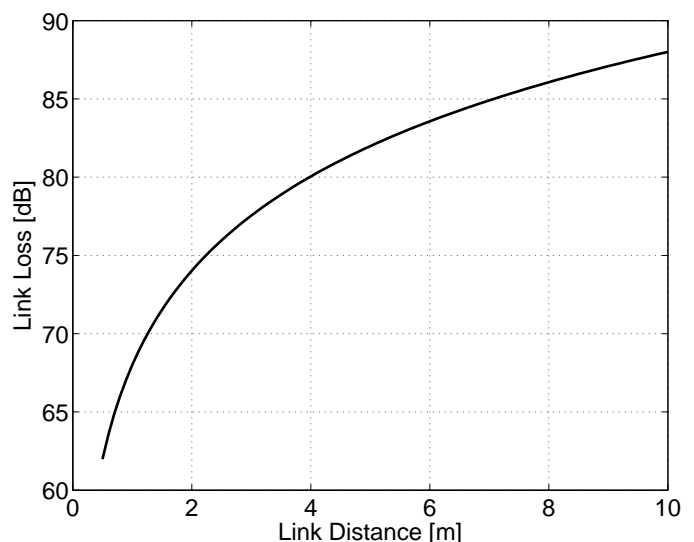


Fig. 1: 60GHz Link loss according to Friis prediction for an isotropic radiator and receiver [1]

examples of 60GHz receiver front-ends in both 0.13 $\mu m$  [4], [5], [6] and 90nm [7] technologies have also been reported. The potential for lower cost and higher integration (e.g., higher packing density for digital circuits at the latest CMOS technology node) for CMOS relative to BiCMOS make it the preferred technology for a consumer application. With deep sub-micron CMOS devices now offering transit frequencies well above 100GHz, there is a strong motivation to focus research in this area on CMOS implementations. However, the choice of technology also influences the eventual transceiver architecture, because many of the common receiver architectures cannot be implemented effectively in all technologies.

## II. SWITCHING-QUAD MIXER

Supply restrictions for deep sub-micron technologies (e.g, 90nm, 65nm) render common topologies such as the full Gilbert cell mixer hard to implement, due to the lack of headroom  $V_{DD} \leq 1V$ . This active mixer topology found in common RF literature [8], contains  $g_m$  state (common source amplifier) with a tail current source cascoded to a

switching quad (see Fig. 2). Trying to apply this topology with  $V_{DD} = 1V$  and  $V_{TH} \approx 0.4V$ , will restrict the drain source to  $V_{DS} \leq 0.2V$ . Working at such low drain-source voltage will exhibit high nonlinear behavior, due to short channel effect, and will degrade the system performance. To avoid these difficulties the Gilbert cell is stripped off his  $g_m$  state, where we are left with the switching-quad. The switching-

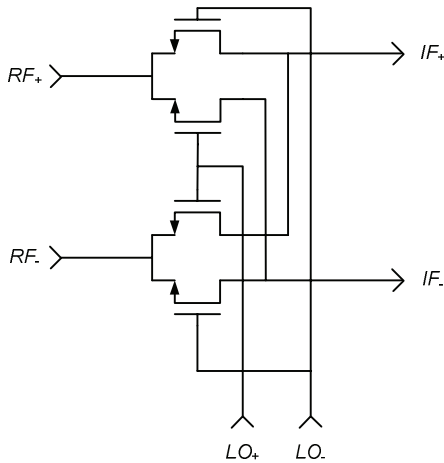


Fig. 2: AC schematic of a switching-quad mixer circuit.

quad can operate in two modes: passive mode, where the drain and source are held at a zero DC potential, and the device operates as a switch. In this mode the  $1/f$  contribution is small and the mixer noise contribution is mainly due to the thermal component. The  $1/f$  noise contribution can be seen in Fig. 3, where the  $1/f$  frequency corner is close to  $1GHz$ , due to the small size of the device. The small size devices ( $90nm \times 5\mu m$ ) are required, so the input capacitance at the LO port will be small enough to ensure the desired LO swing for proper operation, without burning to much power in the LO buffers.

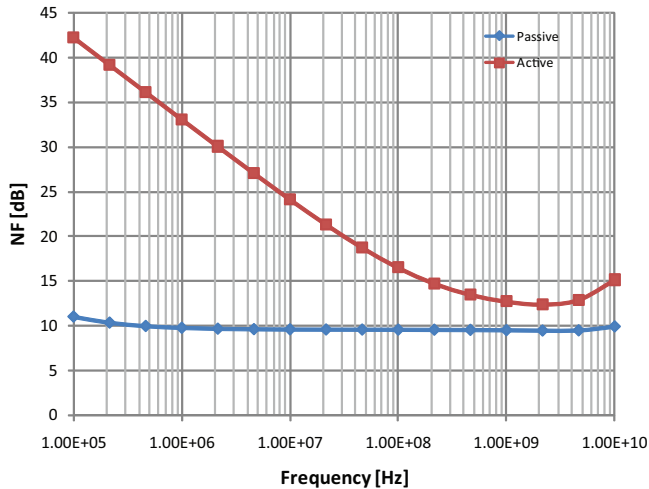


Fig. 3: A switching quad mixer noise figure for active (biased) and passive mode. Device size is  $90nm \times 5\mu m$ .

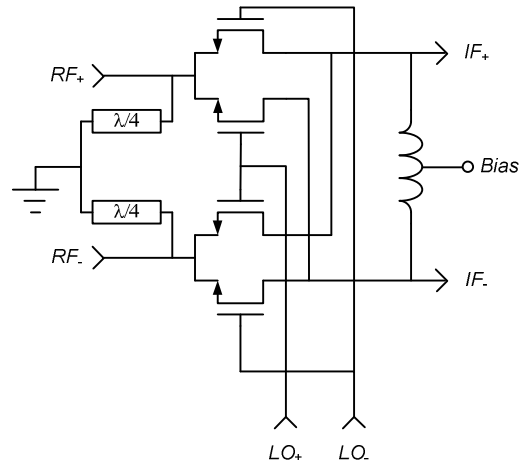


Fig. 4: A biased switching-quad configuration, the drain (IF) is usually connect to the supply voltage, but maybe biased with a different volatge to optimize the system performance.

The second option is a biased (active) mode, in which the drain is connected to the supply voltage (see Fig. 4). The high noise contribution is traded off for ability to work with lower LO amplitudes that require less power consumption in the LO buffers. This is seen in Fig. 5, where one can observe that the active mixer reaches the peak conversion gain at lower LO amplitude than the passive configuration. Moreover, the absolute conversion "gain" of this configuration is higher.

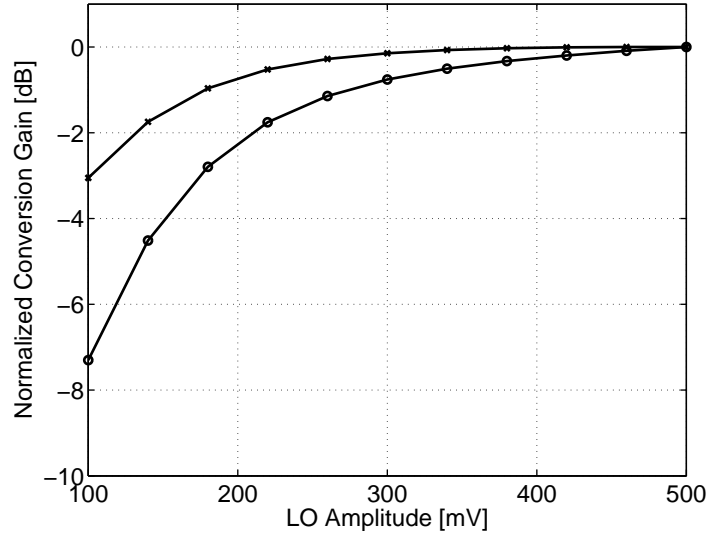


Fig. 5: The effect of the LO amplitude on the mixer conversions gain. The active mixer reaches full gain with lower amplitude than the passive one

### III. SLIDING IF ARCHITECTURE

Combining the switching-quad configurations that were reviewed in the previous section, one can optimize a system both for power consumption and for good noise performance. The sliding IF downconversion architecture, seen in Fig. 6, is such an optimization. Choosing the IF at  $\sim 10GHz$  moves the signal out the  $1/f$  noise, and thus allows the RF mixer

to operate in biased mode. It enables to reduce the size and current consumption of the LO buffers, which due to the high frequency are one of the main current consumers. The IF mixer is operating in passive mode, to reduce its noise contribution. The IF LO buffers operate at lower frequency thus consume less power.

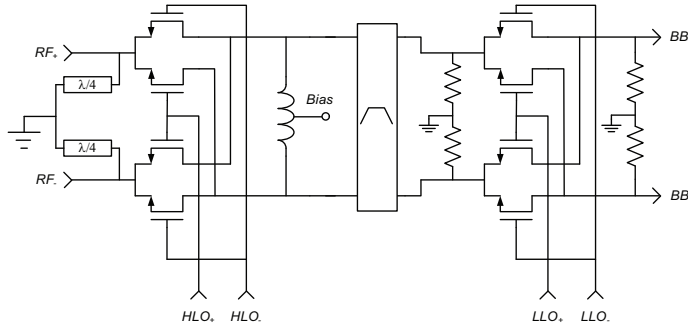


Fig. 6: Sliding IF downconversion system. The first mixer is biased for low current consumption from the RF-LO buffers, and the second mixer is operating in passive mode to avoid  $1/f$  noise contribution.

Another advantage of the this system compared to direct downconversion is that the LO frequency is lower, which makes it easier to generate. Furthermore, the quadrature phase, which is needed for complex detection, is created at the IF frequency, using a frequency divider or with another frequency scheme. Again this is a power saving configuration.

#### IV. IF FILTERING

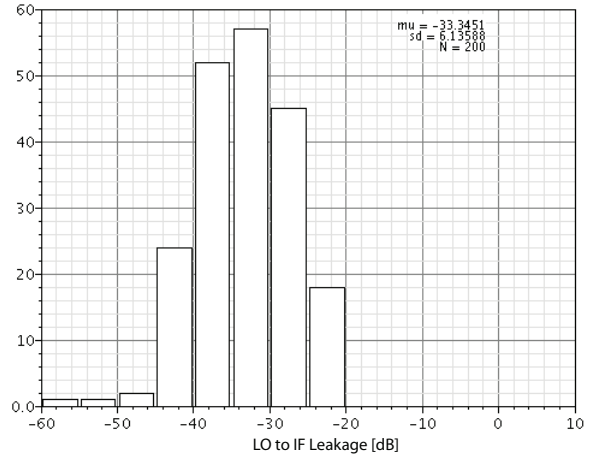
The main drawback of heterodyne architecture for system on chip implementations, is the design of the IF filter. The strict bandwidth specifications and the use of large size components such as the inductors, capacitors and resistors, render it impossible to implement on chip, and usually was implemented off chip, on the printed circuit board. However, it is a different case for 60GHz systems. Observing the frequency plan in table II, it clearly seen that the high IF frequency allows use of relatively small components. Also, due to the oxygen absorption interferers pose less of a problem and thus the filter specification can be relaxed.

TABLE II: Frequency Plan

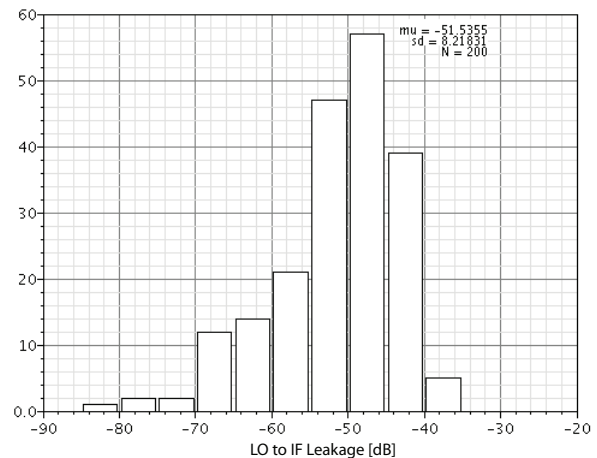
	$IF = \frac{1}{3}RF$	$IF = \frac{1}{5}RF$
RF Freq	60 GHz	60 GHz
RF-LO Freq	40 GHz	48 GHz
IF Freq	20 GHz	12 GHz
LO to BB Leakage	LO-2IF	LO-4IF

From the previous discussion one might wonder if there is a necessity for the IF filter. The need for filtering arises from the LO leakage to the IF, which is then downconverted into the baseband and results in distortion. The two mechanisms of LO leakage are also shown in Table II. The LO leakage results from mismatches during fabrication process, and also due to layout constraints. It can be easily understood that the 12GHz

IF frequency plan is less susceptible to LO leakage to the baseband. However, since the second mixer stage is passive, the models are not accurate enough to predict the effect on the baseband (see further).



(a)



(b)

Fig. 7: Monte-Carlo simulation results of LO to IF leakage for 12GHz frequency plan, both for a biased mixer (a) and for a passive mixer (b). Simulations are performed with equivalent LO amplitudes for both circuits. Transistor sizes are 90nm X 5 $\mu$ m.

This problem is illustrated in Fig. 7. Here the mixer circuit ( four 90nm X 5 $\mu$ m FETs) was simulated using Monte-Carlo simulator for device mismatch, in both passive and biased modes, with equivalent LO amplitudes. It can be observed from the results that the passive circuit exhibits a much higher isolation. However since the model accuracy is poor for  $V_{DS} \leq 0.3V$ , the passive circuit results are questionable.

Even with less isolation the IF filter only needs to block the unwanted LO leakage, and therefore can relaxed. If an IF amplifier is used, the output matching circuit can meet filtering specifications.

## V. CONCLUSIONS

The sliding IF architecture allows the design to be optimized, for both low power consumption and low noise performance. The LO leakage and IF filtering are easily solved if a high IF frequency is selected and if there is a lack of strong interferers.

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