

# A 79GHz Receiver Front-End for Automotive Radar in 90nm CMOS

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**Abstract**—This paper presents a 79GHz receiver front-end designed in a 90nm CMOS process. The front-end consists of a differential low noise amplifier (LNA) intended for an on-chip differential dipole antenna, and a down-conversion mixer. Pseudo-differential structure minimizes the effects of down-bonding on stability, power gain, and noise/power matching performance. Series microstrip transmission line extends circuit bandwidth by resonating with the transistors' gate capacitance. decoupled current biasing of the Gilbert cell based mixer optimized voltage gain and LO drive specifications. Simulations predict an overall power gain of 27dB at 79GHz with a  $-3$ dB bandwidth of 10GHz. Input matching is better than  $-10$ dB in the pass-band and noise figure is 9.4dB at an IF frequency of 100MHz.

**Index Terms**—Receiver front-end, Automotive radar, Millimeter-wave, Low noise amplifier, Mixer, 79GHz.

## I. INTRODUCTION

Millimeter-wave (mm-wave) receiver front-ends find applications in broadband wireless local area networks in the 60GHz ISM band that are currently being defined by the IEEE 802.15.3c task group [1][2], and automotive collision avoidance radar sensor operating between 77 and 81GHz in Europe [3][4]. With the continuous scaling of silicon based CMOS devices, the transistor transit frequency ( $f_T$ ) and minimum noise figure ( $NF_{min}$ ) becomes competitive with the counterparts based on gallium arsenide (GaAs) or indium phosphide (InP) materials. The advancement of multi-level copper interconnects and the availability of thick analog metals also favours the performance of high Q passive magnetics, counteracting the degradation from the semi-conductive silicon substrate. This presented receiver front-end realized in 90nm CMOS technology enables the co-integration of digital signal processing blocks for a low cost solution.

The block diagram of the mm-wave receiver front-end is shown in Fig. 1. It consists of an on-chip antenna, a differential LNA, a double balanced mixer, and a 79GHz phase-locked loop (PLL). At 79GHz, the  $\lambda/4$  wavelength in

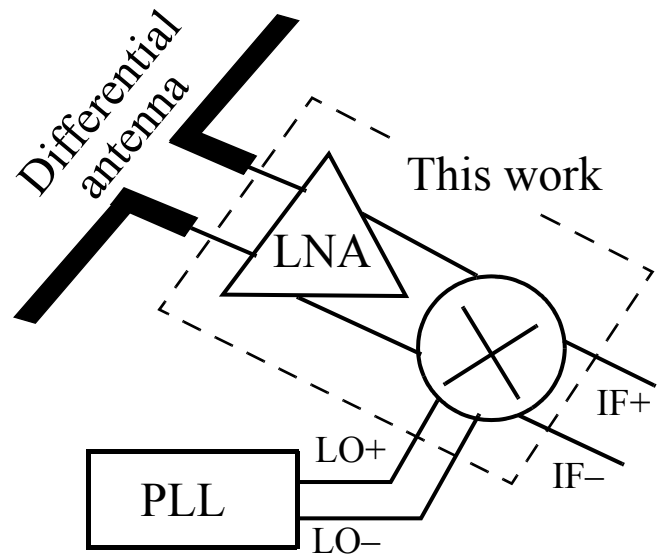


Fig. 1 Block diagram of 79GHz receiver front-end

free space is about 1mm, which would be further reduced in the silicon or silicon dioxide environment due to the higher permittivity of the material. The short wavelength allows the implementation of on-chip antenna, which is on the same substrate as the receiver circuit [5][6]. This simplified the interconnection from the antenna to the receiver pre-amplifier. The differential dipole structure demonstrates a high antenna gain of  $-8$ dB<sub>i</sub> at 24GHz [7]. The antenna drives a differential LNA and directly down-converts to a IF frequency of 100MHz by a double balanced mixer. A PLL, running at 79GHz, drives the mixer LO port at 0dBm.

This paper presents the design and simulation results of a 79GHz receiver front-end in a 90nm CMOS technology. Different design techniques are utilized for optimizing circuit performance at 79GHz, including pseudo-differential structure, virtual grounding, series microstrip resonance, and bias current de-coupling. The overall receiver power gain is 27dB, with a  $-3$ dB bandwidth of 10GHz. The noise figure is 9.4dB at an IF frequency of 100MHz and the LNA input is matched to the  $50\Omega$  antenna at better than  $-10$ dB in the pass-band.

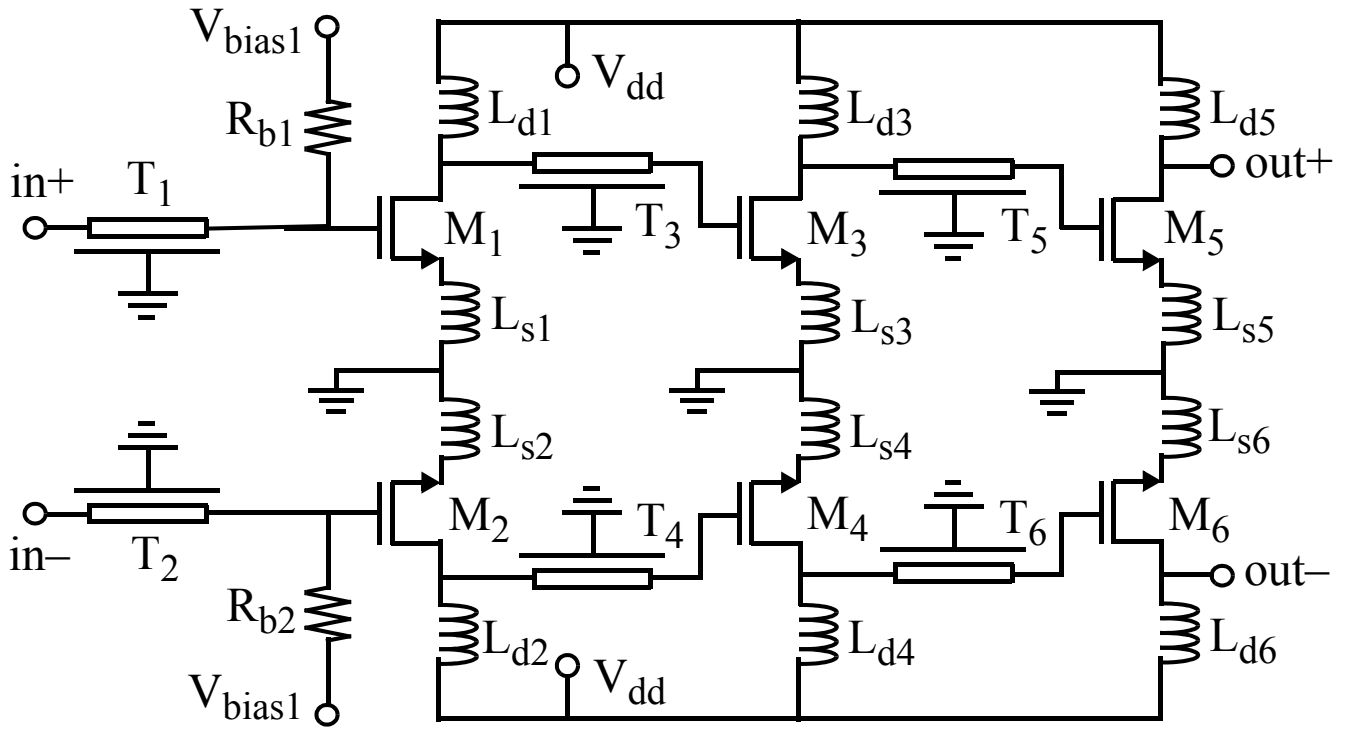


Fig. 2 Schematic of the 79GHz pseudo differential low noise amplifier

## II. LNA DESIGN

High performance LNA has been developed using silicon germanium (SiGe) BiCMOS process [8] which utilizes the low noise, high  $f_T$  SiGe-based heterojunction bipolar transistor (HBT). To design a 79GHz LNA in a 100GHz  $f_T$  CMOS technology, different design techniques have been used. The schematic of the LNA is shown in Fig. 2, which is an improved version of the design in [9]. With a standard 1.0V supply voltage, no cascode topology could be used for higher gain and better reverse isolation. To maintain >10dB power gain in 79GHz, three amplifier stages are in cascade, with each of them as a simple common source NMOS transistor. Each transistor is degenerated with inductor  $L_{s1-s6}$  for improved linearity. Load inductors  $L_{d1-d6}$  resonate with the drain parasitic capacitances for tuned gain. The first amplifying stage is biased at  $V_{bias1}$  for better noise/gain trade-off while the second and third stages are biased at  $V_{dd}$  for simplicity.

Differential structure generates an on-chip virtual ground for differential signaling. This minimizes the effects of down-bonding on the LNA stability, power gain, and input noise/power matching. Virtual ground also eliminates the parasitic oscillation while the coupling between alternative bondwires around an amplifier stage forms a closed loop. As seen in Fig. 2, a pair of three stage amplifiers ( $M_{1,3,5}$  and  $M_{2,4,6}$ ) form a pseudo-differential configuration. This creates a virtual ground at the middle point of  $L_{s1}$  and  $L_{s2}$ ,  $L_{s3}$  and  $L_{s4}$ ,  $L_{s5}$  and  $L_{s6}$ . Pseudo differential shows better linearity performance compared to the conventional differential design technique.

In the mm-wave regime, the interconnects between different stages could no longer be modelled by a simple wire but have to consider the distributed effects. In the presented LNA circuit, the connections are made via microstrip transmission lines  $T_{3-6}$ . The signaling path is the top metal layer while the second layer is used for the ground return path. The lowest metal is reserved for the routing of biasing currents. The microstrip line also forms a series resonant tank with the transistor gate parasitic capacitance. This extends the circuit bandwidth when the line's effective inductance resonates with the gate's capacitance at the operating frequency. Transmission line  $T_{1-2}$  is for the input noise/impedance matched to the 50 $\Omega$  antenna.

## III. MIXER DESIGN

The mixer shown in Fig. 3 is a modified version of the standard double balanced Gilbert type mixer. It down-converts the RF signal from the LNA to an IF frequency of 100MHz. A high IF is chosen to get rid of the high 1/f noise of the CMOS transistors. The bias current of the switching quad  $M_{1-4}$  is decoupled from the input transconductance stages  $M_{1-2}$  by capacitor  $C_{1-2}$ . Thus, the biasing point of the two components could be optimized independently. For a Gilbert type mixer, the parasitic capacitance at the common source node induces signal losses for the RF signal. This losses becomes enormous in the mm-wave range. Similar to the LNA design, an on-chip differential microstrip line is in series with the common source node of the switching quad. This resonates out the parasitic capacitance for higher mixer gain. A differential line is chosen to comply with the compact layout of  $M_{1-4}$ .

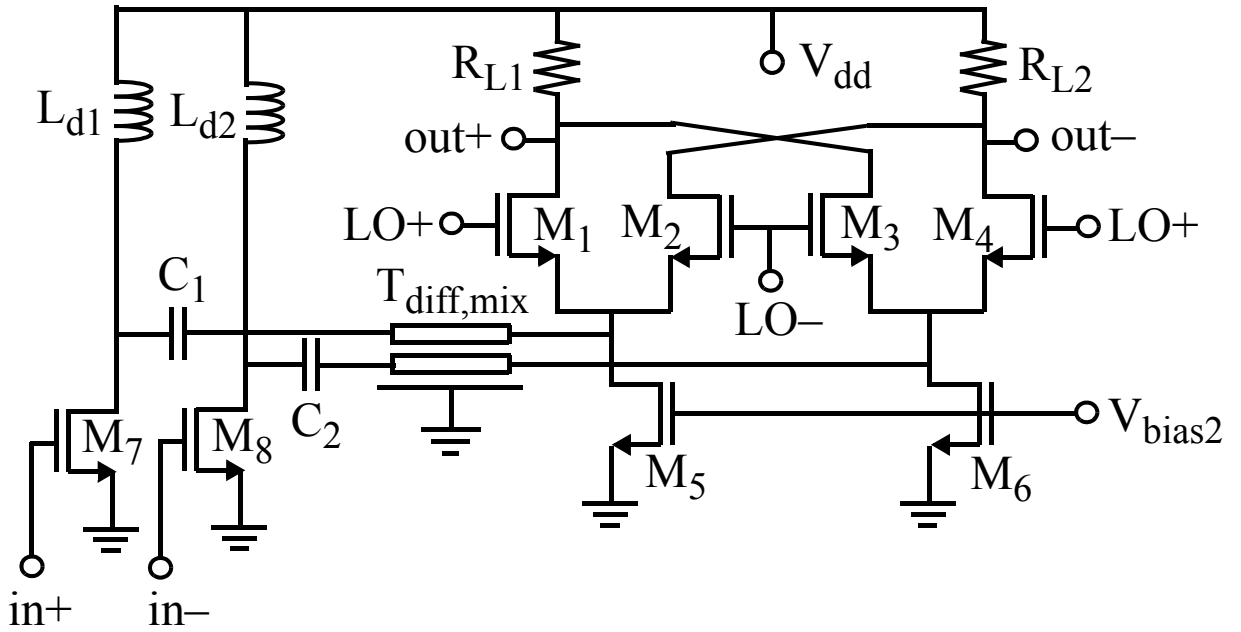


Fig. 3 Schematic of the 79GHz down-conversion mixer

#### IV. SIMULATION RESULTS

The input matching of the receiver is measured by the S-parameter of the LNA input port. The simulated input matching is better than  $-10\text{dB}$ , reference to  $50\Omega$ , from 74 to 84GHz. Noise figure of the LNA reaches the minimum value of 4.2dB and the receiver noise figure is shown in Fig. 4 versus the IF frequency. The mixer flicker noise corner is around 200MHz. With an IF frequency of 100MHz, which results from the trade-off between flicker noise and required bandwidth of the baseband digital signal processing, the noise figure is 9.4dB.

Third order intermodulation is simulated with two frequency tones at 78 and 79GHz being applied at the receiver input. Fig. 5 shows the simulated first and third order output intermodulation products. The input IP3 is  $-18.2\text{dBm}$ . A separated simulation on the receiver linearity gives a  $-1\text{dB}$  compression point of  $-28.4\text{dBm}$  at a supply voltage of 1V.

The receiver power gain and the corresponding RF bandwidth is simulated by varying both the RF and LO frequencies while fixing the IF at 100MHz. Fig. 6 shows simulated power gain of 27dB at 79GHz with a  $-3\text{dB}$  bandwidth of 10GHz. This wideband performance fully satisfied the 79GHz automotive radar requirement for an ultra-wide-band signaling of 4GHz bandwidth.

Table 1 summarizes the presented work and compares the results to previously published 60 and 77GHz receivers front-ends. The presented receiver gives a higher operating frequency and lower noise figure than [1] with a similar conversion gain, though using a finer technology node. As seen from Table 1, CMOS design gives inferior performance to SiGe design [2][6] both in terms of power gain and noise figure.

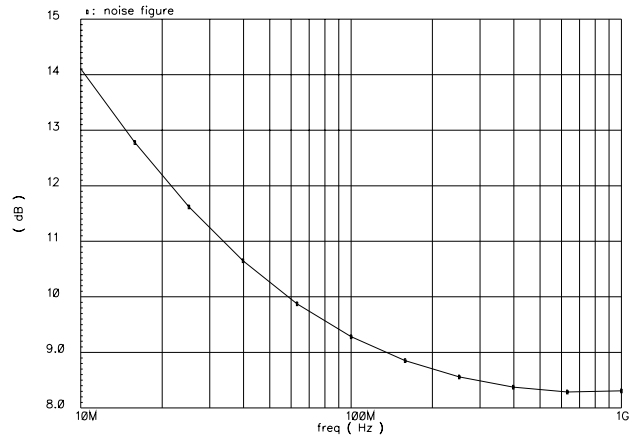


Fig. 4 Noise figure versus IF frequency

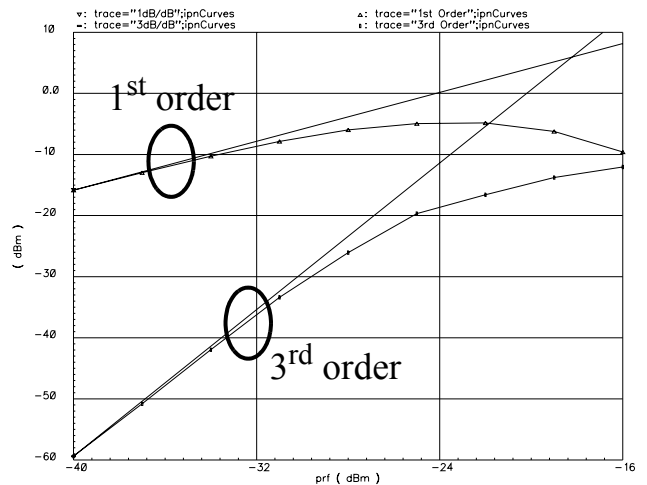


Fig. 5 First and third order inter-modulation products

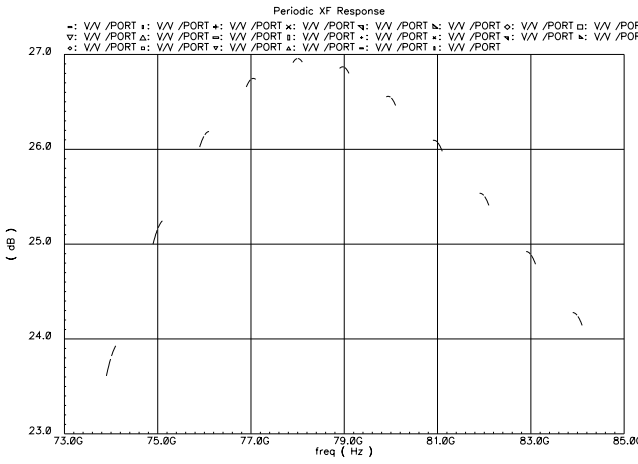


Fig. 6 RF bandwidth with varying RF and LO frequencies

## V. CONCLUSION

A 79GHz receiver front-end is designed and simulated in a 90nm CMOS process. Techniques including pseudo-differential structure, virtual grounding, series microstrip resonance, and bias current de-coupling are utilized for optimum performance in the mm-wave frequency range. Proposed to be integrated with an on-chip differential dipolar antenna, the differential LNA and down-conversion mixer gives a power gain of 27dB with a  $-3$ dB bandwidth of 10GHz. The noise figure is 9.4dB at an IF frequency of 100MHz. Linearity performance gives an input  $-1$ dB compression point of  $-28.4$ dBm and an input third order intercept point of  $-18.2$ dBm. The circuit operates in a supply voltage of 1V.

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Table 1: Performance summary and comparison with state-of-the-art receiver front-ends

|           | Frequency (GHz) | Conversion Gain (dB) | Noise Figure (dB) | Supply Voltage (V) | Input $-1$ dB Compression Point (dBm) | Technology        |
|-----------|-----------------|----------------------|-------------------|--------------------|---------------------------------------|-------------------|
| This Work | 79              | 27                   | 9.4               | 1.0                | $-26.4$                               | 90nm CMOS         |
| [1]       | 60              | 28                   | 12.5              | 1.2                | $-22.5$                               | 0.13 $\mu$ m CMOS |
| [2]       | 60              | 40                   | 6.7               | 2.7                | $-36$                                 | 0.13 $\mu$ m SiGe |
| [6]       | 77              | 37                   | 8                 | 2.5 and 3.5        | Nil                                   | 0.13 $\mu$ m SiGe |